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MODEL 920-D
LOGIC ANALYZER

OPERATING AND SERVICE MANUAL

MP MASTER

MA34610

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GOULD

OPERATING AND SERVICE MANUAL

MODEL 920-D

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SECTION I

GENERAL INFORMATION

1.1 Certification

Gould Inc. certifies that this instrument accessory was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Gould Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Inc. prepaid and Gould Inc. will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF GOULD INC.'S WARRANTY, GOULD INC. SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD INC. BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3 Instrument Description

The Model 920-D Logic Analyzer is a compact, portable, solid-state electronic instrument that has been designed to discriminate logic signal levels against an internal preset threshold and store these discriminated levels in a memory. The memory, once filled, presents the data in the familiar timing diagram format on a CRT display or oscilloscope. The memory may be thought of as a time window, the length of which is a product of the clock interval selected and the number of storage locations present.

1.4 Specifications

SIGNAL INPUTS

Number. Nine; eight dedicated signal inputs and one auxiliary. Auxiliary channel may be used as a ninth signal input, a trigger qualifier, or an external clock qualifier.

Impedance. 1 MΩ , 15 pF nominal.

Threshold. Selectable TTL (+1.4 V), ECL (-1.3 V). Variable + 3 V via potentiometer and test point. Selector switch for X1 or X10 input probes attenuates both fixed and variable thresholds.

Maximum Voltage. ± 50 V peak-to-peak.

Input Modes. SAMPLE. Unit stores the detected input logic level on all channels simultaneously at the active clock edge. LATCH. Unit detects and stores any pulses narrower than one clock period, regardless of their time relation to the clock edge. Minimum pulse always captured is 15 ns wide at the threshold, with a swing above or below the threshold of 500 mV.

TIME BASE AND MEMORY

Clock Interval. INTERNAL. Selectable 0.05 μs to 50 μs in a 1, 2, 5 sequence. EXTERNAL.

Any rate from DC to 20 MHz. Input impedance 1 MΩ, 15 pF. QUALIFIER. External clock may be qualified by the AUX input. A clock will only be gated into the unit when the signal applied to AUX is in the selected state.

Memory. Nine bits by 256-word static RAM. First 248 words are displayed.

ARM FUNCTION

Manual via front panel switch; in Auto Delay mode, unit arms itself after eight display frames.

TRIGGER FUNCTION

Source. INTERNAL. Via combinational trigger switches, user can define a unique parallel bit combination or word from which to trigger unit. Switches allow for a selection of ONE, ZERO, or DON'T CARE (X) level for each input, with respect to selected threshold. AUX input may be used as a qualifier, giving a 9-bit trigger word. Ninth trace then shows trigger point as a positive transition, rather than showing data. EXTERNAL. Via rear panel TRIG IN BNC connector, TTL level, positive edge. Input is ANDed with internal combinational trigger; TRIG IN may be used as a trigger word extender by using a 10-TC Probe Pod. Trigger word can then be up to 19 bits wide.

Manual. Via front panel switch.

Output. TRIG OUT BNC provides negative-going TTL level signal each time the trigger word is detected. May be used as a scope sync.

Delay. CLOCK. When trigger word is detected, unit counts clock intervals selected by Trigger Delay thumbwheel. When count is complete, unit starts (Delay) or stops (Pretrigger) recording. Selectable to 9990 clock intervals. EVENT. When trigger word is detected, unit counts each occurrence of subsequent trigger words, until count is complete. Unit then starts (Delay) or stops (Pretrigger) recording. The Nth trigger word is at the beginning (Delay) or center (Pretrigger) of memory. Selectable to 999 events.

RECORD MODES

Delay. Unit is armed manually or automatically, allowing it to accept a trigger. Recording begins at trigger or after trigger delay (clock periods or events) is counted out. Recording ceases after memory is filled with new data. When in Delay Auto mode, unit arms itself after display of eight frames of data, and is ready for another trigger.

Pretrigger. Recording begins when unit is armed, and stops when trigger occurs or after trigger delay is counted out. When trigger delay is in terms of clock periods, trigger event is positioned N clock periods before end of memory.

When trigger delay is in terms of trigger events, the Nth trigger is centered in memory.

DISPLAY OUTPUT

X Output. Repetitive 1 V p-p ramp, period of 512 μs.

X Expand. X5 (X-ramp slope increased by 5); maximum amplitude approximately +3 V.

Y Output. Repetitive 4608 μs stairstep ramp; each step 512 μs duration. Data for each channel modulates each respective step. Full range nominally 0 to +1 V.

Z Output. Nominal 0 to +3.5 V pulse, 12 μs duration occurring every 512 μs synchronously with X-ramp. Z Output. Nominal +3.5 V to 0 V pulse, otherwise as above.

MISCELLANEOUS

Size.	HEIGHT.	6 in. (15.2 cm).
	WIDTH.	10.5 in. (26.7 cm), including bail.
	DEPTH.	17.25 in. (43.8 cm), including rear panel feet.

Weight. 9.5 lbs. (4.3 kg).

Power. 100, 115, 200, 230 VAC ± 10%; 32 W, 50-400 Hz.

Temperature Range. 0-50°C, operating; convection cooled.

10-TC Provision. Power output and trigger input for one 10-TC Probe Pod.

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model 920-D.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Gould Inc., Biomation Division, representative or the Gould Inc., Biomation Division, factory.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice. A factory approved shipping carton can also be obtained by contacting Gould Inc., Biomation Division.

2.4 Power Connection

The 920-D may be used on a wide range of power line voltages. Two rear panel switches allow for selection, as noted in Table 2.1. The unit will operate at the voltages shown within + 10%, and line frequencies from 50 to 400 Hz.

Table 2.1. Line Voltage Selection

DESIRED VOLTAGE	LINE Switch	VOLTS Switch
100	LOW	115
115	NORM	115
200	LOW	230
230	NORM	230

NOTE: When VOLTS switch is in the "115" position, use a 1-A slow blow fuse; in the "230" position, use a 1/2-A slow blow unit.

2.5 Preparation for Use

The Model 920-D can be operated in a self-contained system by simply connecting it to a CRT display oscilloscope. The following sections of this manual cover operation and setups.

2.6 Initial Warm-up

Although the Model 920-D is a solid-state instrument, a brief warm-up period of approximately 10 minutes is required for the internal circuitry to reach thermal stabilization.

SECTION III

OPERATION

3.1 Introduction

This section identifies and describes front panel controls, rear panel connections, and typical operating procedures. Included are complete descriptions of front panel controls and their effective ranges, location and proper use of rear panel connectors, and a step-by-step procedure for using various modes of the instrument. A thorough understanding of this section is essential to the successful use of the instrument.

3.2 Front Panel Controls and Connectors

This section includes descriptions of the various front panel controls and how they affect the operation of the instrument. These controls are discussed in a logical sequence of operations required to set up the machine to record signals. In each case, the nomenclature appearing at the switch is used to identify that switch.

See Figure 3.1.

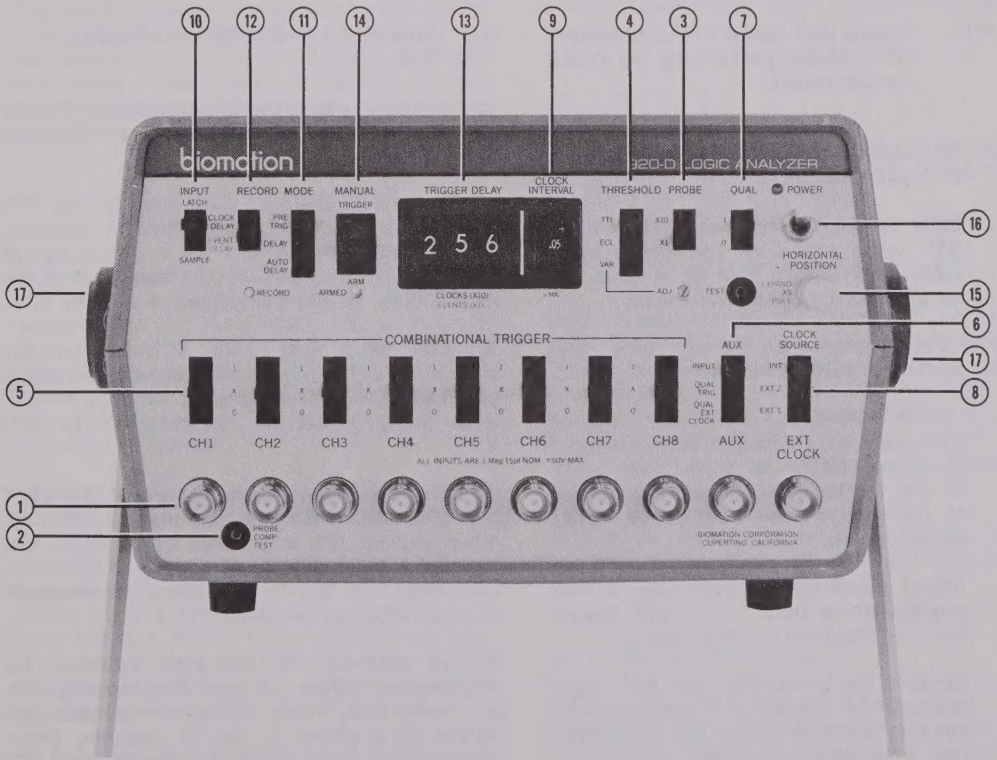


Figure 3.1 Front Panel Functions

(1) INPUTS

Ten BNC connectors. Eight of these connectors are used for signal inputs. The ninth channel, AUX, is a multipurpose input. The tenth input is for the external clock. All inputs are 1 MΩ, 15 pF nominal impedance. Maximum input voltage without damage is ± 50 V.

(2) PROBE COMP TEST

This test jack allows for properly compensating a given compensatable probe to the input impedance of the 920-D. This test point is connected directly to Input Channel 1.

To compensate a given probe proceed as follows:

NOTE: Ensure that Model 920-D is powered up before performing the probe compensation.

a. Connect the probe to be compensated to Input Channel 1.

b. Using an oscilloscope, connect another X10 scope probe to the oscilloscope input, and ensure that it is properly compensated to the oscilloscope.

c. Connect the probe tip of this second probe to PROBE COMP TEST point.

d. Connect the probe tip of the original X10 probe (connected to Input Channel 1) to the Calibrate signal test point of the oscilloscope. Obtain a display of the square wave calibration signal on the scope.

e. Adjust compensation capacitor of the original probe until the proper square wave is observed on the scope.

f. Replace the probe that was just compensated to any of the channels, and connect another probe for compensation to Channel Input 1.

g. Repeat this procedure until a sufficient number of probes have been compensated for the logic analyzer.

(3) PROBE X10/X1

This switch allows for attenuation of the selected threshold by a factor of 10, so that when using X10 probes at the inputs, the threshold selected is with respect to the probe tip. In the X10 position, the threshold selected is attenuated internally by a factor of 10. In the X1 position, the threshold is not attenuated.

Note that this switch not only affects the preset threshold, but also the adjustable threshold.

(4) THRESHOLD TTL/ECL/VARIABLE, ADJ/TEST

The switch and adjustment potentiometer allow for the selection of various input thresholds to the logic analyzer.

When the THRESHOLD switch is in the TTL position and switch (3) is in the X1 position, the threshold selected is + 1.4 V. When switch (3) is in the X10 position, the threshold at the input BNCs of the instrument is + 0.14.

When switch (4) is in the ECL position and switch (3) is in the X1 position, the threshold selected is -1.3 V. Likewise, when switch (3) is in the X10 position, the threshold is -0.13 V.

By using the ADJ potentiometer and the TEST point, an adjustable threshold may be selected. When switch (3) is in the X1 position, the threshold is variable between ± 3 V; when switch (3) is in the X10 position, the threshold may be adjusted between ± 0.3 V.

If you wish to use the logic analyzer for considerably higher voltages than those provided, note that, if a X10 probe is used and switch (3) is placed in the X1 position, thresholds of up to ± 30 V are available at the probe tip.

(5) COMBINATIONAL TRIGGER

Each of the eight input channels has associated with it a combinational trigger switch. This three-position switch allows you to select an edge from which to trigger. If all switches are in "X" or "DON'T CARE" position except one, that channel will be the triggering channel. For instance, if we place the combinational trigger switch for Channel 1 in the ONE position, then the instrument triggers on a positive-edge signal applied to Channel 1.

More importantly, the set of switches allow you to select a parallel bit pattern from which to trigger the instrument. Once a desired bit pattern is selected and the instrument is armed, it watches for that bit pattern in the input signals. Once that bit pattern is detected, the instrument triggers.

The input signals are compared against the combinational trigger circuitry after the input signals have been latched inside of the instrument. Thus, captured glitches as narrow as 10 ns also help to satisfy the combinational trigger word.

(6) AUX INPUT/QUAL TRIG/QUAL EXT CLOCK

This three-position switch controls the function of the auxiliary input. In the INPUT position, the auxiliary input acts as a ninth data channel. As such, it may be used for recording parity bits on an 8-bit-plus-parity system. When used in this fashion, this input has no influence over the combinational trigger word selected.

When this switch is in the QUAL TRIG position, the auxiliary input may be used as the trigger qualifier. In this case, switch (7) is used to select the state of the auxiliary input that is used to qualify the combinational trigger. Thus, even though the eight input channels match the combinational trigger word selected, the 920-D does not derive a trigger from this event until the auxiliary input also matches its qualifier state.

By using the Model 10-TC Probe Pod Accessory, the combinational trigger word can be extended up to 19 bits. The Model 10-TC provides for a 10-bit extension of the combinational trigger word. For detailed information on this accessory, contact Biomation.

When switch (6) is in the QUAL EXT CLOCK position, a signal may be applied to the auxiliary input that causes any externally applied clock to be gated by this signal. For instance, let us assume that you have placed switch (7) in the ONE position, and you have further connected a signal to the auxiliary input. Whenever this signal is a logic one level, the 920-D accepts any external clock applied. The signal applied to the auxiliary input, in effect, controls the information that is being recorded by the 920-D.

This capability is useful for those occasions when you wish to choose specific words from a data stream. You may select a signal within your system that allows you to pick out only the information that you wish to view or only certain information when a particular circuit is active.

(7) QUAL 1/0

This switch operates on the auxiliary channel when switch (6) is either in the QUAL TRIG or QUAL EXT CLK positions.

(8) CLOCK SOURCE INT/EXT ∫ /EXT ⌇

This switch controls the source of the record clock for the 920-D. When in the INT position, the clock interval is that selected by switch (9). When in either of the EXT positions, the instrument accepts an external clock via the EXT CLOCK input. Strobing of the input data into memory can be selected for positive- or negative-edge clocking.

Only when you have selected an external clock source can the auxiliary input (6) be used as a clock qualifier.

(9) CLOCK INTERVAL μs

This switch allows you to select a convenient clock interval with respect to the data that you wish to record and examine. To get the total record window covered by the memory, multiply the clock interval selected by 256.

Available clock intervals are as follows: 0.05, 0.1, 0.2, 0.5, 1, 2, 5, 10, 20, and 50 µs.

The clock interval selected controls the time resolution of the data recorded. For instance, if we select an interval of 0.05 µs, we are able to see our recorded information with a time resolution of 50 ns.

(10) INPUT SAMPLE/LATCH

In the Sample input mode, the instrument strobes its inputs simultaneously at whatever interval is selected by switch (9). The state of the input signal at that instant in time is recorded in memory. If any signals or glitches occur that are less than one clock period in width, the instrument neither detects nor records these pulses, unless the pulse occurs at the sampling edge of the clock.

However, when in the Latch position, the instrument not only records data signals every clock interval, but is also capable of detecting and capturing any signals or glitches that are less than one clock period in width. If a pulse exceeds the selected threshold by 500 mV, it need only be 15 ns wide at the threshold to be detected and captured.

This latch feature is important, not only to capture random pulses in the signal, but also to detect and record desired signals in a data stream.

For instance, consider a case where you are looking at a sequence of events in a machine that covers a rather long span of time, say 10 ms. By selecting the 50 µs clock interval, the 920-D spans a time window of approximately 12.8 ms. Consider further that some of the signals the system you are examining have pulses with a duration of just a few microseconds. The clock interval is fixed by virtue of the timing sequence of the system and the time window required to cover it. By using the Latch input mode, these narrow pulses can be detected and captured, and then displayed with the other signals in the system. Without the Latch input mode, these pulses could not be recorded.

Both positive-going and negative-going pulses are captured with the Latch input mode.

(11) RECORD MODE PRETRIG/DELAY/AUTO DELAY

In the Delay position, the 920-D is armed via switch (14). Arming the instrument allows it to seek and detect a trigger event. Once the trigger event is detected, the unit begins filling its memory with new information. When the memory has been filled, the instrument goes into a display sweep. The information captured is held and displayed until the unit is armed and accepts a trigger event. After the trigger is detected, a new block of data appears on the display to replace the old.

The Auto Delay position works the same as the Delay position, with the exception that the unit is armed automatically after the unit has displayed its memory contents eight times.

In the Pretrig position, the instrument is capable of capturing both prior trigger and post trigger information. Once the unit is armed, it begins recording information; when a trigger is detected, it stops recording and goes into a Display mode. Thus, all information in the memory of the instrument is prior trigger information. If switch (13) is used to delay the trigger event, then both prior trigger and post trigger information is recorded (see also the information for switch (13).

(12) RECORD MODE CLOCK DELAY/EVENT DELAY

When in the Clock Delay position, the unit counts the number of clock intervals set on switch (13). When the switch is in the Event Delay position, the unit counts trigger events instead of clock intervals.

(13) TRIGGER DELAY
CLOCK (X10)/EVENTS (X1)

When switch (12) is in the Clock Delay position, the number set here is the number of clock intervals that are counted by the unit before the trigger event is acted upon. The count selected here begins when the combinational trigger event is detected.

When the unit is operating in the Delay record mode, is armed, and the trigger event is detected, the unit counts the trigger delay out. At the end of the trigger delay count, the unit begins recording; recording ends when the memory has been filled with new data.

If you select the Pretrigger record mode and arm the unit (switch (14)), recording begins. When the unit detects the trigger event, clock interval countdown begins. When the count is complete, the unit stops recording. If the trigger delay is less then 250, both pretrigger and post trigger information is recorded.

For instance, setting a trigger delay of 010 means that 100 clock intervals are recorded after trigger. Thus, 156 clock intervals of information are saved prior to trigger.

Note that the number selected by the trigger delay switches, when switch (12) is in the Clock Delay position, is multiplied by 10. Thus, in Figure 3.1 the number 256 on the thumbwheels is 2,560 clock intervals of trigger delay.

When switch (12) is in the Event Delay position, the Trigger Delay is in terms of trigger events. Now the unit counts combinational trigger events instead of clock intervals. The first trigger event detected after arming starts the count. Excluding this first event, the unit counts down the number of events selected by switch (13). Thus, in Figure 3.1, selecting a delay of 256 means that the unit counts down 256 combinational triggers before recording starts (Delay) or stops (Pretrigger).

When operating in the Delay mode, the unit counts combinational trigger events between arming and the beginning of recording. In the Pretrigger Record mode, the unit begins recording upon being armed. It continues recording and counting trigger events. When the trigger delay is counted out, the unit continues to record for one-half of the memory length. Thus, in Pretrigger Record Event Delay mode, the unit saves half of its memory before and half of its memory after the Nth combinational trigger event.

The ability to count combinational trigger events is very helpful. For instance, when troubleshooting a handshake digital interface, we can actually count the number of flag-command interchanges that occur at the interface and look at information at any desired point during the data transfer. Thus, if we wish to look at the time relationships on various control and data lines after the 13th handshake, it is easy for us to do so by counting the flags being returned by the peripheral. We can then capture information that occurs in the vicinity of the 13th flag.

(14) MANUAL TRIGGER/ARM; RECORD, ARMED LEDs

Pressing switch (14) down arms the instrument. The ARMED LED lights up. If the unit is in Pretrigger record mode, as selected by switch (11), the RECORD LED also lights up. If operating in the Delay record mode, and the combinational trigger event occurs, the record light illuminates or blinks.

Pressing switch (14) up manually triggers the instrument. The manual trigger is an override to any other triggering. The manual trigger also times out with respect to the trigger delay selected.

By manually arming and triggering the unit, a random burst of signals may be acquired from the system being observed.

(15) HORIZONTAL POSITION EXPAND X5 PULL

This is a combination potentiometer and switch. When the knob is pushed in towards the panel, no expansion of the display occurs, and the position control has no effect on the display.

When the knob is pulled out, the display is expanded by a factor of 5 horizontally. The potentiometer can then be used to position the display so that the entire memory contents may be viewed in increments of approximately 50 clock intervals. When the position control is pushed back in, the display automatically centers itself.

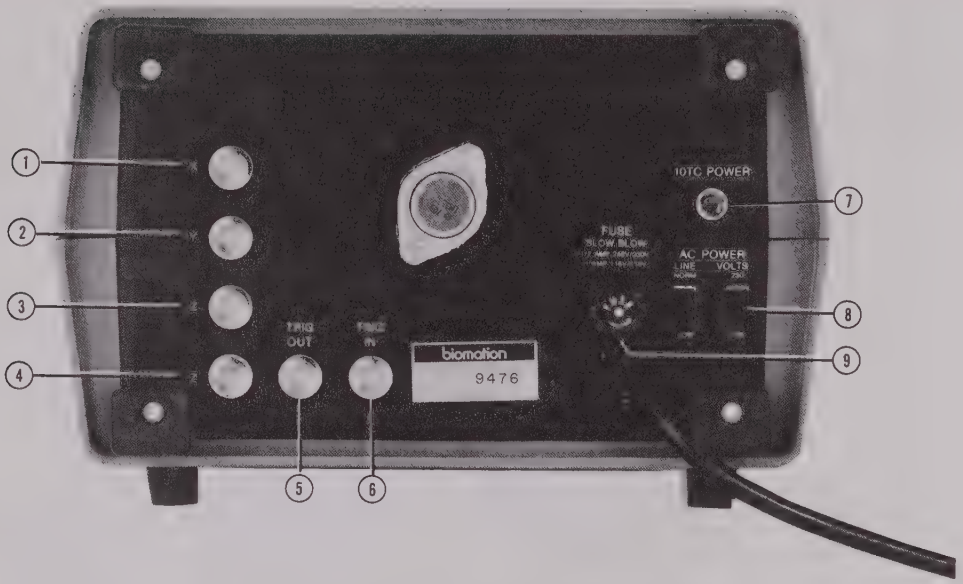


Figure 3.2 Rear Panel Functions

This control has no effect when the horizontal axis of the display device is not being driven by the logic analyzer (X Output, function (1), Section 3.3).

(16) POWER

The switch controls AC power to the instrument, and the red LED indicates when power is applied.

(17) BAIL CONTROL

The large plastic knobs on each side of the instrument are used to control the bail position. By pulling out these knobs, the bail can be rotated to any of six different positions. When the desired position is found, press both knobs inward towards the cabinet; this locks the bail in that position.

3.3 Rear Panel Functions (Refer to Figure 3.2)

(1) X Output

Provides a repetitive 1 V p-p ramp. The period is 512 μs. This signal is used to drive the horizontal of the display device, and must be used to provide axis for expansion and positioning of the traces with switch (15).

(2) Y Output

Provides a repetitive stairstep ramp; each step is 512 μs in duration. Data for each recorded channel modulates each respective step. Full range of this signal is nominally 0 to +1 V.

The above signals are adjustable over a nominal range. Refer to Section V for the procedure.

(3) Z Output

The signal here is a nominal 0 to +3.5 V pulse, 12 μs wide, and occurs every 512 μs. The falling edge of this pulse is synchronized with the beginning of the display sweep.

This signal may be used to blank a simple X-Y CRT display (for those displays requiring a positive level blanking signal), or to trigger the time base of an oscilloscope for display synchronization.

(4) $\overline{Z}$ Output

This signal is the negation of the Z Output; the pulse is +3.5 V to 0 V at a 12 μs duration. The rising edge of the pulse is synchronized to the beginning of the display sweep.

(5) TRIG OUT

The output here is a TTL high level at all times, except when the instrument detects the combinational trigger event. At that point, a negative-going pulse is output. This pulse is output each time the instrument detects the trigger event.

This output is useful for synchronizing a scope sweep with the combinational trigger circuitry. In this fashion, you can observe actual waveforms in a particular data stream with the scope by triggering it with a precisely defined combinational trigger word.

(6) TRIG IN

This input is TTL compatible, and is active on the leading edge of a pulse applied. The primary intention of this input is for compatibility with the Model 10-TC Probe Pod.

(7) 10-TC POWER

This connector provides power for the Model 10-TC Probe Pod. On pin 1, the output is +5 V at 360 mA; pin 2, -5 V at 100 mA; pin 3, ground.

The mating plug for this connector is a LEMO, part number F-0303-NYLU3.2.

(8) AC POWER

The two switches, LINE and VOLTS, are used to select the proper operating line voltage. Refer to Table 3.1 for proper switch positions. The 920-D functions properly at line voltages +10% from the values in the table, and at line frequencies from 50-400 Hz.

(9) FUSE

Use a 1-A slow blow fuse for nominal 115 VAC; use a 1/2-A unit for nominal 230 VAC.

3.4 Set-up Procedure and Operation

3.4.1 Initial Set-up

This section describes the connection of the Model 920-D with a CRT display or oscilloscope.

Before connecting the unit to line power, check that the voltage selector switches are set properly (see Table 2.1) and that the correct size fuse (as printed on the rear panel) is installed.

Connect the 920-D to a pulse generator with manual, single-pulse capability, and a CRT or oscilloscope. See Figures 3.3 a and b. Depending upon the particular CRT or oscilloscope used, it may be necessary to use the $\overline{Z}$ output of the 920-D for the retrace blanking signal.

CAUTION: Some older "tube-type" oscilloscopes have high voltage levels on their Z axis inputs. This could damage the Z or $\overline{Z}$ outputs of the 920-D. Please check before connecting the unit.

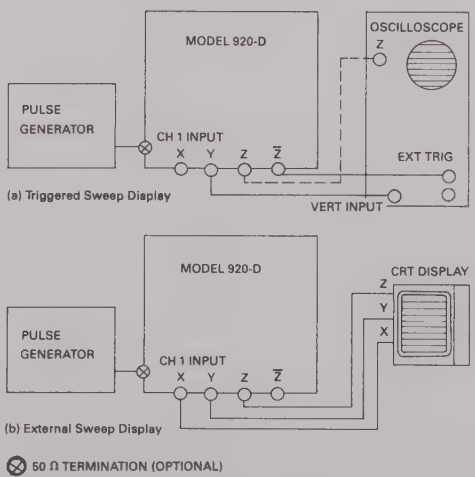


Figure 3.3 Display Interconnections

Set the units (where appropriate) as follows:

Oscilloscope/CRT

Vertical Sensitivity	~0.1 V/div, DC coupled (Figures 3.3 a, b).
Vertical Position	Nine traces evenly spaced on display (Figures 3.3 a, b).
Horizontal Sweep	50 μs/div (Figure 3.3 a).
Horizontal Sensitivity	0.1 V/div, DC coupled (Figure 3.3 b).
Trigger Input	Negative slope, DC coupled, external input (Figure 3.3 a).

Pulse Generator

Output	Single, manually triggered pulse, 2.5 μs wide, 0 to +3 V amplitude.

920-D Logic Analyzer

Input Mode:	Sample
Record Mode:	Clock Delay Pretrigger
Trigger Delay:	003
Clock Interval:	0.1
Clock Source:	Internal
Threshold:	TTL
Probe:	X10
Combinational Trigger:	CH 1-"1", CH 2 through 8- "X", AUX-"Input", QUAL-"0"

Adjust vertical and horizontal positioning controls to center the nine-trace display.

3.4.2 Operation

This section demonstrates the following modes of operation: Input Sample, Input Latch, Clock Delay Record, Event Delay Record, Pretrigger Record, and Delay Record.

3.4.2.1 Input Sample and Pretrigger Record Modes

Press MANUAL ARM. The 920-D's ARMED and RECORD LEDs light, indicating the unit is recording and awaiting a stop trigger event defined by the COMBINATIONAL TRIGGER. Pulse the generator. The 920-D receives the trigger, delays 30 clock intervals (TRIGGER DELAY), and stops recording. Figure 3.4 shows the display. Channel 1 displays the pulse while Channels 2 through AUX remain low. The TRIGGER DELAY chosen (003) allows the trigger pulse to be viewed. A TRIGGER DELAY OF 000 stops the 920-D from recording at the trigger event and does not record the pulse. A TRIGGER DELAY of 012 (120 CLOCK INTERVALS) gives the display shown in Figure 3.5. Note that 136 clock intervals of prior trigger data and 120 clock intervals of post-trigger data are displayed.

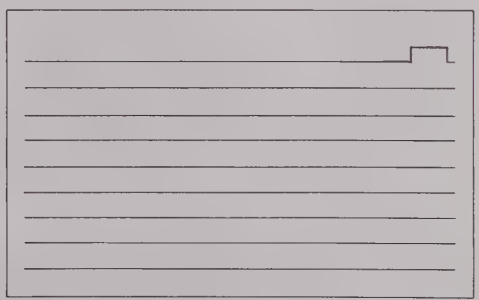


Figure 3.4 Sample, Pretrigger Record Mode With A Trigger Delay of 30 Clock Intervals

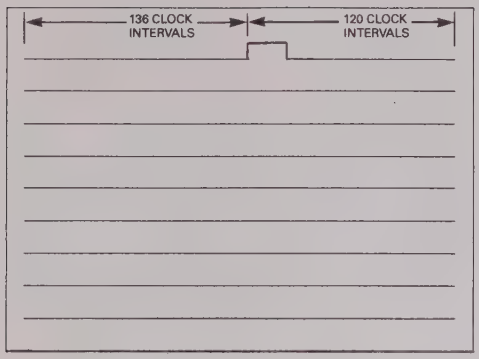


Figure 3.5 Sample, Pretrigger Record Mode With A Trigger Delay of 120 Clock Intervals

3.4.2.2 Input Sample and Delay Record Modes

The Delay record mode can be demonstrated by switching the three-position Record mode switch from PRETRIG to DELAY. Change TRIGGER DELAY to read 000. Press MANUAL ARM. The ARMED LED lights, indicating the 920-D is ready to record at the detection of a COMBINATIONAL TRIGGER event. Pulse the generator. The 920-D receives the trigger event and records until the memory is full. Figure 3.6 shows the pulse on Channel 1. The data shown in Figure 3.6 is post-trigger data. By using the TRIGGER DELAY, additional post-trigger information can be recorded.

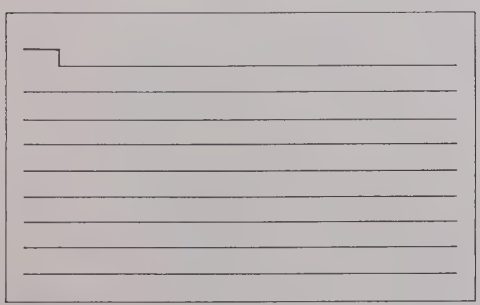


Figure 3.6 Sample, Delay Record Mode

3.4.2.3 Input Latch and Pretrigger Record Modes

Move the three-position Record mode switch from DELAY to PRETRIG. Set the TRIGGER DELAY to 012. Set the Clock Interval switch to 20 μs. While in INPUT SAMPLE, press MANUAL ARM and pulse the generator. The 920-D triggers and displays only if the leading edge of the internal clock coincides with the high state of the pulse. With a 20 μs clock interval and a 2.5 μs pulse, it can take as many as ten pulse repetitions for this coincidence to occur.

Select INPUT LATCH. Press MANUAL ARM and pulse the generator. The 920-D captures the generator's pulse every time. The captured pulse is represented on Channel 1 of the 920-D (to the right of center) with a 1 clock interval pusle (20 μs). The LATCH feature is particularly useful for detecting narrow, random noise pulses or "glitches". The ability to detect narrow pulses is independent of the CLOCK INTERVAL. In the Latch mode, the 920-D can detect pulses as narrow as 10 ns.

3.4.2.4 Event Delay and Pretrigger Record Modes

Select INPUT SAMPLE. Move the two-position Record mode switch from CLOCK DELAY to EVENT DELAY. Set the TRIGGER DELAY to 005. Press MANUAL ARM. The ARMED and RECORD LEDs light, indicating the 920-D is recording. Pulse the generator six times. On the first generator pulse the ARMED LED extinguishes and the 920-D continues to record. The five event delay begins here. The 920-D continues recording 128 clock intervals (half memory) after the sixth generator pulse. Recording stops at that time and the output is displayed. The input pulse is displayed on Channel 1 at the center of the screen.

Note that an EVENT DELAY of 000 while operating in the Pretrigger record mode is valid.

3.4.2.5 Event Delay and Delay Record Modes

Move the three-position Record mode switch from PRETRIG to DELAY. Press MANUAL ARM: ARMED LED lights. The 920-D is ready to record. Pulse the generator six times. On the first pulse, the ARMED LED extinguishes. The event count begins here. On the sixth pulse the 920-D begins recording until the memory is full. The pulse is displayed on Channel 1 at the left side.

Note that an EVENT DELAY of 000 while operating in the Delay record mode is invalid.

SECTION IV

PRINCIPLES OF OPERATION

4.1 Introduction

This section is formatted in two parts. The first part gives a block diagram description of the instrument and explains how it operates in various record and display modes. This part acquaints the user with the instrument and describes how it operates so that the maximum benefit from the use of the instrument may be derived.

The second part of the section gives a detailed treatment of the theory of circuit operations. This section is invaluable for those who wish to understand the in-depth operations of the instrument and for those who wish to service it.

4.2 Basic Functional Description

For the discussion that follows, refer to the block diagram in Figure 4.1.

The Model 920-D Logic Analyzer is an instrument that samples its inputs and compares the voltage levels present at these inputs with an internal reference, called the threshold. The discriminated voltage levels are stored in memory as digital ones and zeros. Once the memory is filled, the information is reconstructed in a timing diagram format and output through a multiplexer to an oscilloscope or CRT Display.

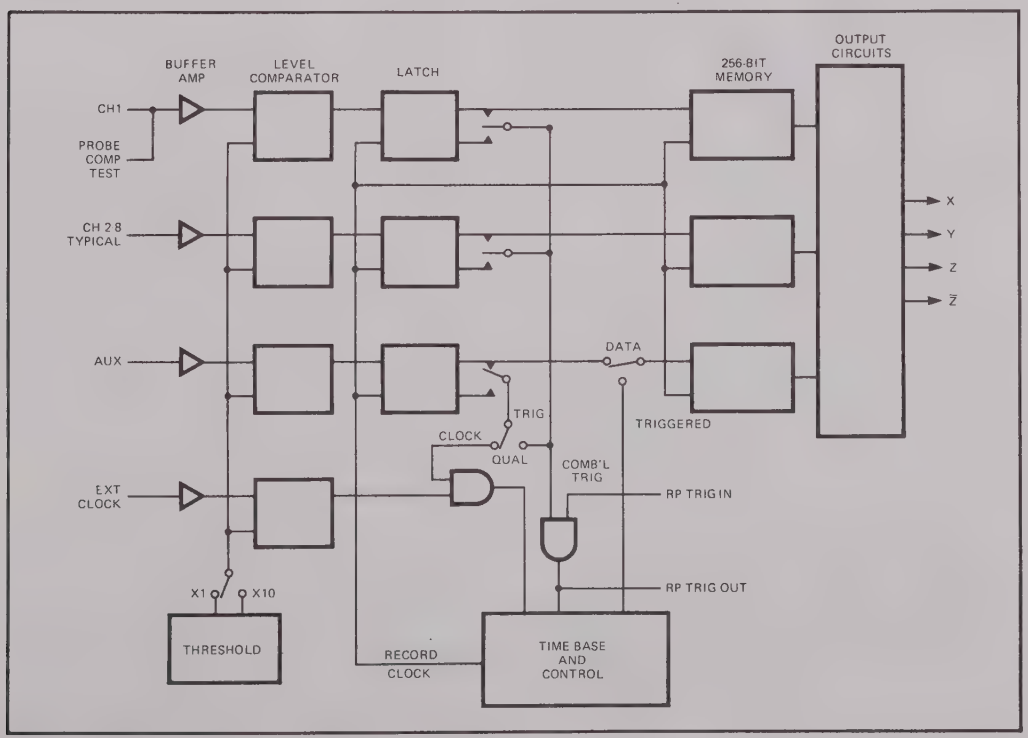


Figure 4.1 920-D Block Diagram

It is convenient to think of the memory of the logic analyzer as a "time window." By selecting appropriate combinational trigger events and using the trigger delay capabilities of the instrument, this "time window" may be positioned at virtually any desired point with respect to the data of your system. In subsequent paragraphs we will look at the ways in which we may position this record window.

First, let's step logically through the block diagram of the instrument.

4.2.1 Inputs

Each of the 10 inputs on the Front Panel has a buffer amplifier associated with it. This gives the instrument a 1 MΩ , 15 pF nominal input impedance that allows you to use virtually all commercially available scope probes, both X1 and X10. The probe should be capable of compensating to an instrument input capacitance of 15 pF. Take care not to apply more than ± 50 V to any one input because this causes damage to the input circuitry.

The probe compensation test point is connected to input Channel 1. Refer to Section III for a description on how to use this test point.

The buffered input signal is then fed to a level comparator. The reference voltage for this comparator comes from the threshold selection circuitry. This takes the form of a three-position switch and variable potentiometer on the front panel. In addition, the threshold reference can be attenuated by a factor of 10, for use with X10 scope probes.

Whenever the input signal level is at a more positive (or less negative) level than the threshold voltage selected, a logic level 1 is stored in the latch circuitry. Whenever the input signal level is less positive (or more negative) than the threshold selected, a logic level 0 is stored in the latch.

4.2.2 Sample Mode

When using the Sample input mode of the instrument, the input levels are strobed into the memory as 1 or 0 levels, based upon the signal level with respect to the selected threshold at the time of the record clock pulse. The Sample mode is typically used for the following conditions:

1. When signals are being recorded in the system under test with respect to a system clock and you want to look at data flow in the system, rather than timing signals.

2. When, for some reason, you wish to look at the signals in the system and disregard glitches that are less than 1 clock period wide.

Note that, because of the way the Sample mode operates, the unit neither detects nor records pulses that are less than 1 clock period wide, unless these pulses happen to be coincident with the active edge of the record clock.

4.2.3 Latch Mode

The Latch input mode allows you to detect and record any pulses that occur on input lines that are less than 1 clock period in width. This is a very valuable input mode for hardware troubleshooting. Both positive- and negative-going glitches as short as 10 ns may be captured with this method, regardless of the clock interval selected on the front panel.

Let's consider a case where you desire a time window sufficiently long to capture a sequence of events in your system. The time window required is on the order of 10 ms. If we divide 10 ms by 250 (the approximate length of the memory), we get a clock interval of 40 µs. The closest clock interval available on the instrument is 50 µs. This gives us a total record window of 12.5 ms.

However, suppose there are signal pulses of approximately 1 µs duration in your circuit that you wish to observe. Note that, in the Sample mode, we are unable to detect and record pulses of that width unless they are coincident with the clock. However, with the Latch mode, we can always be sure of detecting and recording those signal pulses.

The Latch input mode is basically governed by an energy function. Thus, the shorter the pulse, the greater the voltage overdrive required to detect and capture that pulse.

This is illustrated in Figure 4.2. The Model 920-D is capable of capturing a pulse 15 ns wide at the threshold when the pulse amplitude is 500 mV above the threshold.

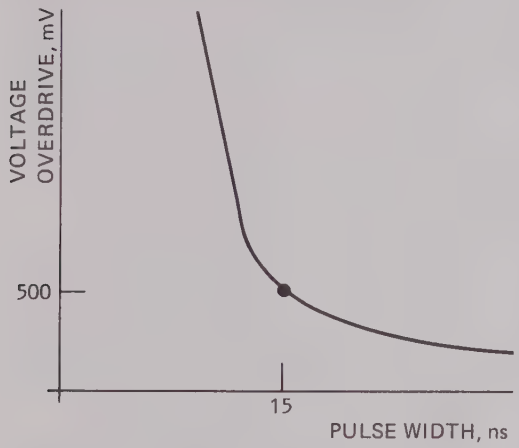


Figure 4.2 Relationship Between Threshold Overdrive and Minimum Pulse Captured

4.2.4 Auxiliary Input

This input gives you a great deal of flexibility in using the 920-D. This input may be used as a ninth signal recording input, or as a qualifier for the trigger word or for the external clock input. These three functions of the auxiliary input are exclusive; when it is used for one function, it cannot be used for any other function.

4.2.5 Record Clock

The 920-D requires a clock to strobe the latch circuitry and to load the data into memory. An internal clock is also used to provide display clocking.

The rate at which data is recorded from the inputs can be controlled either via the internal clock, which is crystal controlled, or via an external clock input on the front panel. In either case, the instrument always reverts to its own internal clock for display output.

The 920-D accepts an external clock rate from DC to 20 MHz. The clock rate selected determines the time resolution of the data that is stored in memory. For instance, if we select a 2 µs clock interval, the information displayed on the screen can be observed with a resolution of 2 µs. Thus, the clock interval is the limiting factor in making timing measurements between signals.

4.2.6 Triggering

The 920-D has some very versatile triggering capabilities. First, by using the auxiliary input as a data input, the user may trigger from an 8-bit wide combinational trigger word. If the optional 10-TC probe pod is connected, you can trigger from an 18-bit combinational word. The auxiliary input, in this case, functions as merely a ninth channel that does not contribute to the combinational trigger.

When using the auxiliary input as a trigger qualifier, the 920-D becomes an eight channel logic analyzer with the ninth channel acting as a trigger marker point. A positive transition on the Channel 9 display marks the trigger event. The signal input to the ninth channel also contributes to the combinational trigger word. Thus, you can trigger from a 9-bit word (or 19-bit word using a 10-TC Probe Pod).

This trigger event only appears in memory when operating in the Pretrigger record mode. Refer to the paragraph below, which explains recording modes.

The combinational trigger detection occurs at the output of the latch circuitry. Thus, when operating the Latch input mode, the combinational trigger need only be valid for a period of 10 ns to be detected. The rear panel trigger input (TRIG IN) is ANDed with the internal combinational trigger.

The rear panel TRIG OUT indication is derived from the ANDing of these two trigger sources. This signal is a TTL level negative-going pulse. The signal may be used to trigger an oscilloscope for observing real-time pulse wave shapes with respect to some combinational trigger pattern.

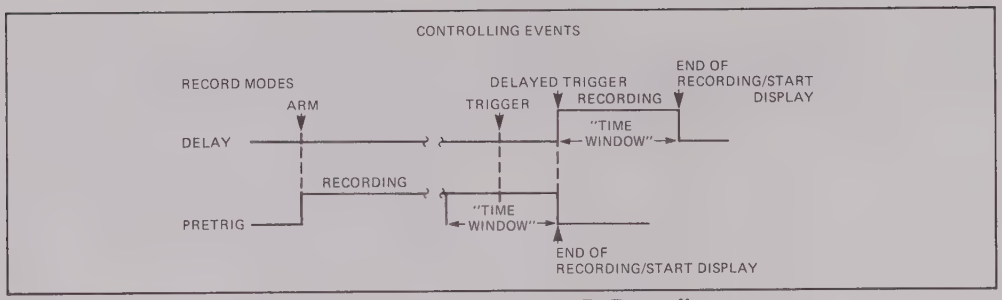


Figure 4.3 Model 920-D Recording Control Functions

4.2.7 Record Modes

The arm and trigger signals control the acquisition of data by the 920-D. Refer to Figure 4.3 above. Recall the concept of the time window, which is represented by the length of the memory and the time per memory cell selected (clock interval). The arm signal must always be issued to the instrument before it can accept a trigger; there are no exceptions to this rule. The arm signal may be applied automatically by operating in the Auto delay record mode. By operating in either the Pretrigger or Delay record mode, you control when the instrument is armed and, therefore, when it can accept a trigger event.

In the Delay record mode, once the unit is armed, it looks for a trigger event. When the trigger event occurs, it starts strobing information from the latch circuitry into memory. It continues strobing data into memory until the memory is filled. Recording then ceases, and display begins automatically. The beginning of recording is delayed by delaying the trigger event. Thus, we have positioned the time window to some point immediately after the trigger, or some delayed time after the trigger.

When we use the Pretrigger record mode, the arm event starts the unit recording. When the trigger event occurs, the unit stops recording. Thus, at that point in time, the time window we have defined is 256 clock intervals prior to trigger. By inserting trigger delay, we can reposition the time window such that the trigger event is somewhere within the memory. In Figure 4.3 we have inserted enough trigger delay so that the trigger event is approximately centered in the memory. Thus, we have both prior trigger and post trigger information.

The concept of pretrigger recording is extremely valuable (and unavailable in an oscilloscope), not only when we wish to observe events that occur in time, but also to look at events that preceded a desired point in time. For instance, we could trigger from a parity error bit and look at the information that occurred prior to that error indication to determine the cause of the error.

The easiest way to remember the functions of the two record modes is as follows: In the Delay record mode, the trigger event starts the acquisition of data; in the Pretrigger record mode, the trigger event stops the acquisition of data. If we remember this statement, the effect of the trigger delay is the same in both cases, and it is then easy to set up the instrument for acquiring data.

4.2.8 Display

Once the memory is filled with data the unit automatically goes into a Display mode, repetitively outputting the memory contents in a fashion that allows display on an ordinary oscilloscope. The data recorded on each channel is sequentially output to the scope, which is why we only need a single vertical input scope or display unit. The data is displayed at a high enough rate so that no flicker occurs on the screen. Expansion in the horizontal direction is provided by a built-in control, provided we are driving the X axis of the display or scope. A horizontal position control allows us to look at the entire memory in approximately 50 clock interval increments.

4.3 Detailed Description

The Model 920-D Logic Analyzer records digital input data to 20 MHz rates. Eight channels record data while a ninth (AUXiliary)

performs one of three roles. AUX acts as either a data input channel, a trigger event qualifier, or an external clock qualifier.

The Model 920-D has two states of operation, either recording data from inputs or displaying data stored in memory. Three operating modes are available in the Record state.

1. Pretrigger Record

2. Delayed Trigger Record

3. Auto Delayed Trigger Record

A programmable delay is used in each record mode. The delay may represent the number of sample clocks or the number of trigger event occurrences.

A general discussion of the record modes follow, focusing on the Machine state and Record Mode Logic. The AUX channel operation is discussed separately as is the Display mode.

4.3.1 Pretrigger Record Mode: Delay by Clock Intervals

Refer to Figures 4.4 and 4.5. Input data signals for Channels 1-8 and AUX are buffered and shaped by input comparators before inputting to 256-bit static RAMs. The combinational trigger monitors only CHs 1-8.

The Record Mode switches select Pretrigger Record, Clock Delay, and AUX while in Input. The operation cycle is as follows.

The manual arm sets ARM FF and the RCD FF. This places the 920-D in the Record mode. Write Enable strobes data into memory. $\overline{\text{RMTC}}$ resets the Memory Tracking Counter.

ARM FF Enable allows Trigger FF to be set by either a manual trigger, combinational trigger, external trigger, or trigger generated from the external trigger pod. ARM FF is reset and the Trigger Delay Counter is enabled.

Trigger Delay Counter, having been preset by the Trigger Delay thumbwheels to the number of samples after the trigger event, now counts down at the time base rate to zero and resets TRIG FF and RCD FF. Until now the Memory Tracking Counter has been held reset. It is now enabled and begins counting up from zero. The zero count represents the point in memory where the last data sample was recorded.

The setting of the Arm FF places the 920-D in the Record state. Setting the TRIG FF establishes the point in time from where the Delay Counter is referenced. The TRIG FF stays set for the length of time programmed via the Trigger Delay Thumbwheel switch. The delay indicates how many samples are taken after the trigger. Programming more than 256 delay intervals will completely destroy all pretrigger information because memories are 256 bits long. In the delay by clock interval operation, 0 to 9990, intervals with a resolution of 10 sample intervals are programmable.

See the timing diagrams in Figure 4.5.

In Pretrigger record mode, the trigger position is displayed on the auxiliary channel when AUX is set either to QUAL TRIG or QUAL EXT CLK. This is represented by a low-to-high transition at the trigger point.

4.3.2 Pretrigger Record Mode: Delay by Trigger Event

Refer to Figures 4.6 and 4.7. In this record mode, several unique operating conditions exist.

1. The Delay Counter counts trigger events.

2. The Trigger Delay Thumbwheel switches represent a number of trigger occurrences, N. The range is 1 to 999 with a resolution of one event.

3. After N+1 trigger events, 128 bits of post-trigger information is recorded.

The Record Mode switches select Pretrigger Record and Event Delay. The operation cycle is as follows.

Manual Arm sets ARM FF and the RCD FF. $\overline{\text{PMTC}}$ is active low, presetting MTC to 128.

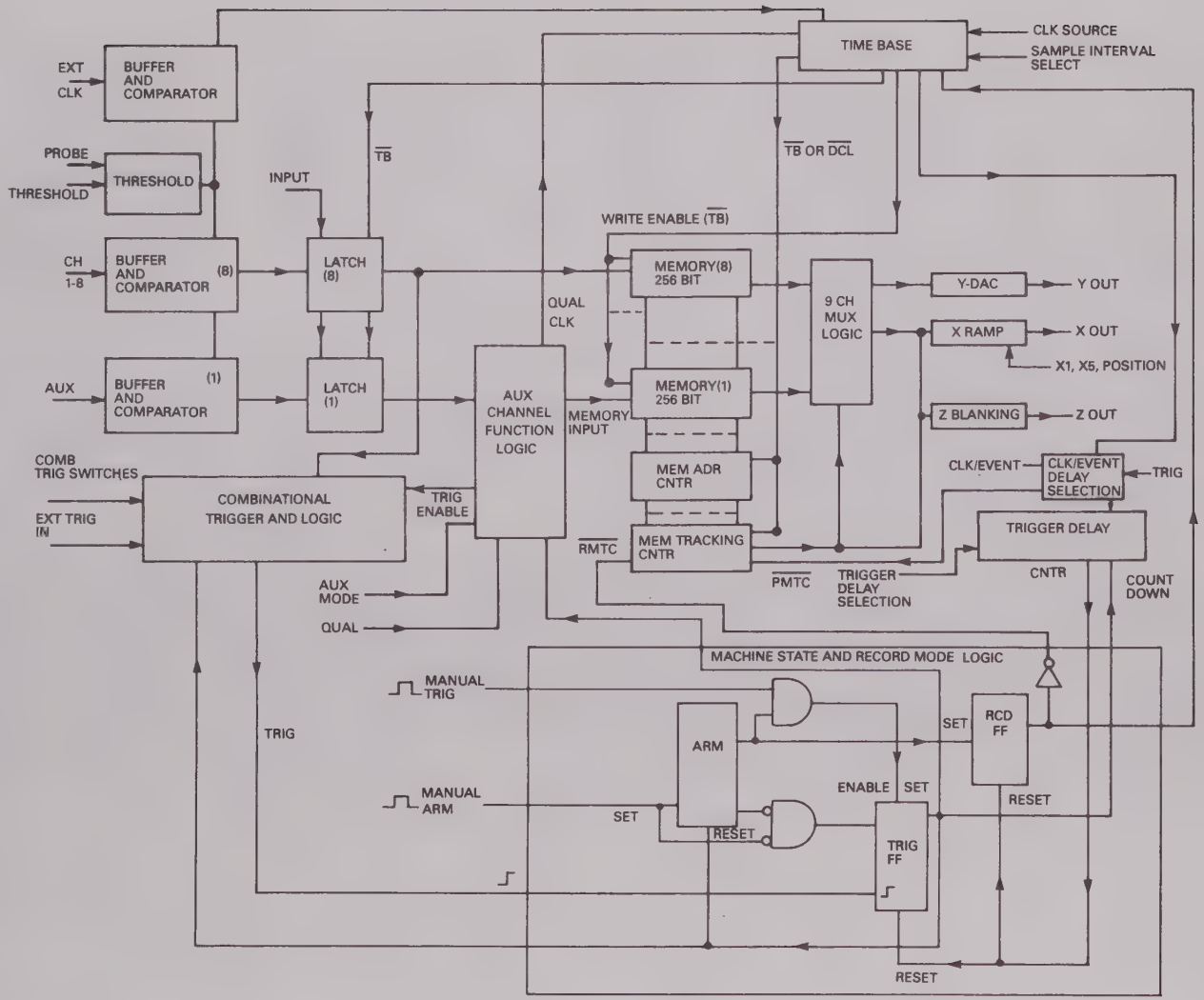


Figure 4.4 Model 920-D Block Diagram in Pretrigger Record Mode/Clock Delay

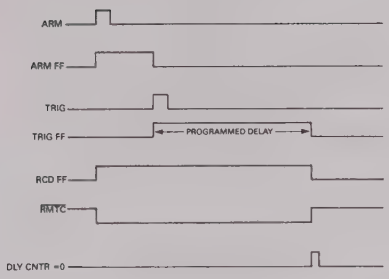


Figure 4.5 Pretrigger Record Mode/Clock Delay

ARM FF Enable allows Trigger FF to be set by either a combinational trigger, external trigger, or trigger from the external trigger pod. ARM FF is reset and the Delay Counter is enabled to count trigger events.

Trigger Delay Counter counts down to zero after N+1 trigger occurrences. Trigger FF is reset and the $\overline{\text{PMTC}}$ signal is removed.

NOTE: The Manual Trigger will not cause the Trigger Delay Counter to be decremented.

Data is recorded for 128 clock samples after the N+1 trigger. When MTC = 0, the Record FF is reset and Display state is entered. The N+1 event appears center screen because the Memory Tracking Counter was preset by $\overline{\text{PMTC}}$ to 128.

The AUX channel will display the TRIG FF (if AUX switch is set to either QUAL TRIG or QUAL CLK). The falling edge of TRIG FF (always occurring at center screen) represents the N+1 trigger event. The rising edge represents the first trigger event after the Manual Arm signal is released.

For N=0, AUX channel will display a pulse at center screen indicating the trigger event. Timing diagrams are shown in Figure 4.7.

4.3.3 Delayed Trigger Record Mode: Delay by Clock Intervals

Refer to Figures 4.8 and 4.9. In this record mode, data is displayed after a specified delay (sample clock intervals) from the trigger point.

The operation sequence is as follows.

Manual Arm sets ARM FF and enables TRIG FF.

TRIG FF is set by either a manual trigger, combinational trigger, external trigger, or trigger from an external trigger pod. ARM FF is reset by TRIG FF. Trigger Delay Counter is enabled and counts down.

Trigger Delay Counter reaches zero, resetting Trigger FF and generating a reset pulse to the Memory Tracking Counter. Record FF is set. Memory Tracking Counter = 0 FF is reset.

Record FF is reset by MTC = 0 after 256 record clocks. Recording ends and data is displayed.

Timing Diagrams are shown in Figure 4.9.

4.3.4 Delayed Trigger Record Mode: Delay by Trigger Events

Refer to Figures 4.10 and 4.11. This record mode counts the Trigger Delay Counter down by the trigger event occurrences rather than by the sample clocks. The operation sequence is identical to the delay by clocks intervals in Step 4.3.3.

Note that the Trigger Delay Thumbwheel switches have a range from 000 to 999, but only 001 to 999 are valid.

For a delay setting of N, the 920-D enters the Record mode after N+1 trigger occurrences.

4.3.5 Auto-Delayed Trigger Record/Delay by Clock Intervals

Refer to Figure 4.12. The operation of this mode corresponds to Delayed Trigger Record with the exception that Arming is performed automatically.

The operation cycle is as follows.

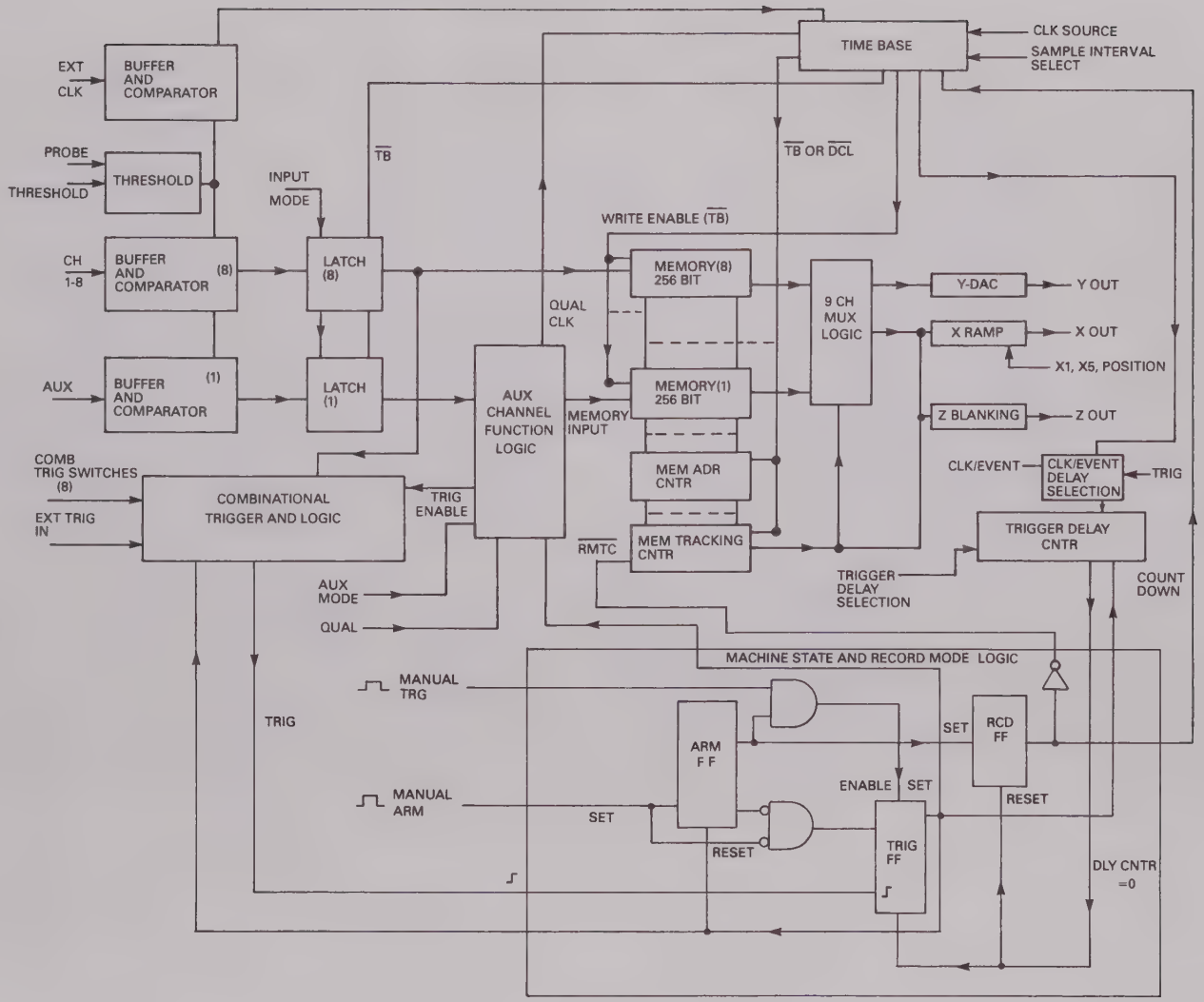


Figure 4.6 Model 920-D Block Diagram in Pretrigger Record Mode/Event Delay

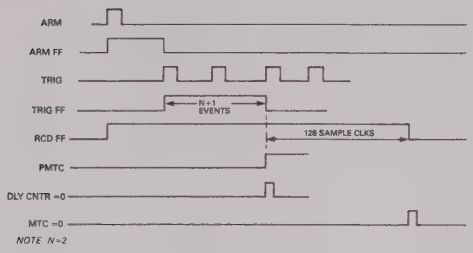


Figure 4.7 Pretrigger Record/Delay by Trigger Event

Selection of the Auto-Delayed mode automatically arms the 920-D and begins Normal Delayed Trigger mode of record.

Data is displayed for eight frames. The Display Counter and Logic then sets ARM FF and the machine waits for a trigger. This display is uninterrupted.

The auto-arming feature constantly updates the memory contents each time a trigger occurs. Thus the display, due to CRT persistence, shows changing or intermittent data.

Timing is identical to Figure 4.7 with the exception that arming is done automatically every eight frames.

4.3.6 Auto Delay Trigger Record/Event Delay

Refer to Figures 4.10 and 4.11. Operation is similar to the Auto Clock Delay mode. The Trigger Delay Counter is decremented by trigger event signals. N+1 trigger events must occur before the RCD FF is set.

Timing is identical to Figure 4.10 with the exception that ARM signals are generated every eight display frames.

4.3.7 AUX Channel Operation

The AUX channel performs one of three functions.

1. Data Input Channel
2. Trigger Qualifier
3. External Clock Qualifier

As an Input channel, AUX functions exactly as CHs 1-8 but does not take part in the combinational trigger. AUX essentially provides a "Don't Care" (X) weight in the combinational trigger.

In the Qualifying mode, trigger or external clock pulses are accepted only when the qualifying signal logic level at AUX matches the QUAL switch level condition, 1 or 0. QUAL TRIG mode displays the trigger event as a 0 to 1 level transition on the CH 9 display position if the QUAL condition is met in the Pretrigger record mode. Trigger event is displayed for both QUAL TRIG and QUAL CLK. In other words, the only time it's not displayed is in Input mode.

Refer to Figure 4.12. Note that two combinationally true triggers were generated. Event 2 caused the TRIG FF to set because only at Event 2 did the signal at AUX match the QUAL condition. With a trigger delay of 12 X 10 = 120 clocks, the trigger event appears just right of center screen. The full display is 250 bits wide and delays are measured from the screen's right edge. For a zero delay, the trigger will not be visible due to CRT blanking considerations. In Auto or Delayed Trigger record mode when operating in either QUAL CLK or in QUAL TRIG modes, the Channel 9 display position will record a zero.

The Qualifying External Clock mode allows the user to choose which clock cycle will write data into memory. The Clock Source switch determines whether the rising or falling edges cause time base transitions. See Figure 4.13 for a typical operation. Note that whenever AUX and the Qualifying condition do not match, Time Base (TB) is low.

4.3.8 Display State Operation

Whenever the RCD FF is reset, the 920-D displays data stored in memory at the Display Clock Rate of 500 kHz. The X, Y, and Z signals are shown in Figure 4.14. Note that for each channel of data, the display is unblanked for 500 bits of data.

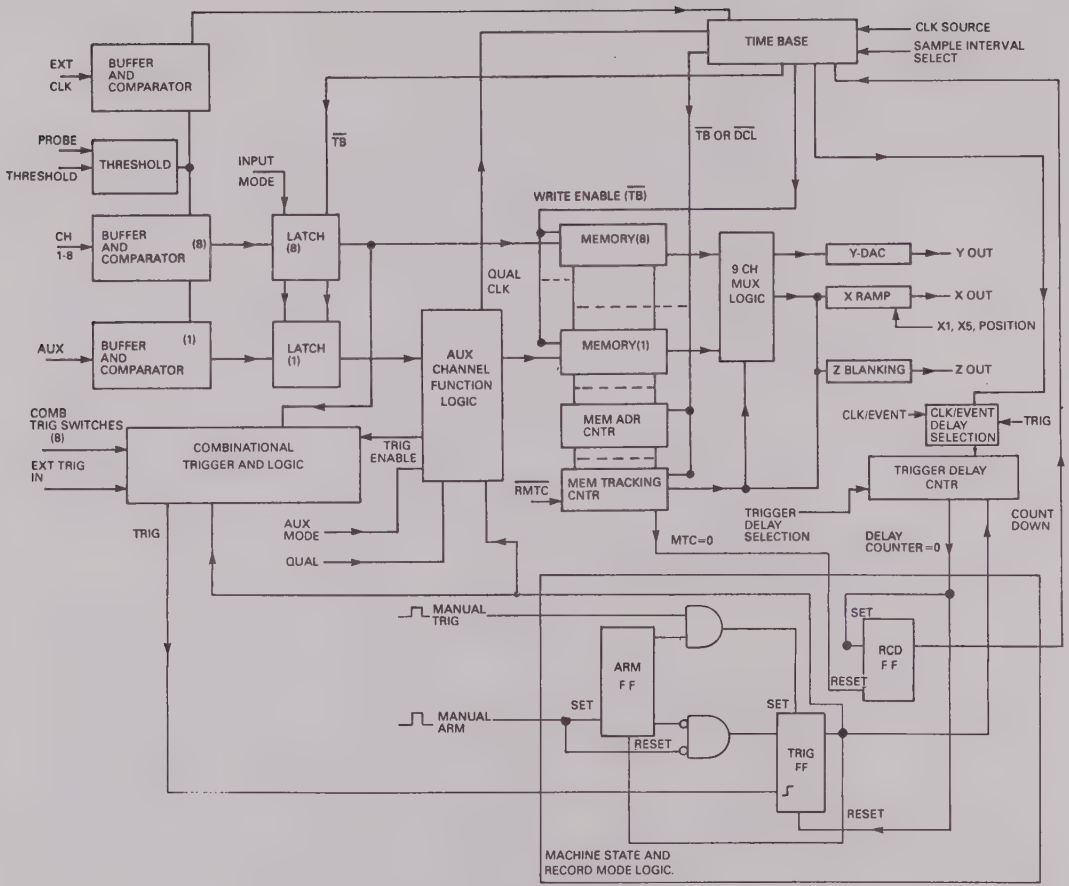


Figure 4.8 Model 920-D Block Diagram in Delayed Trigger Record Mode/Clock Delay

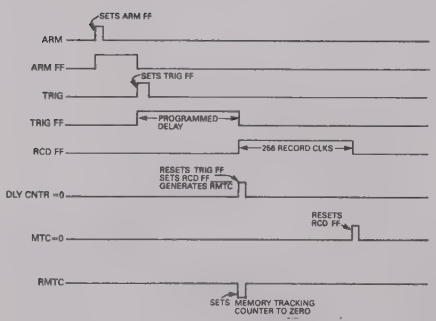


Figure 4.9 Delayed Trigger Record/Clock Delay

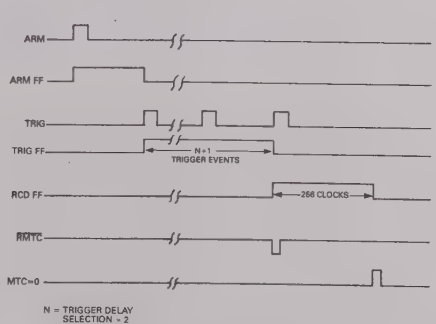


Figure 4.10 Delayed Trigger Record/Event Delay

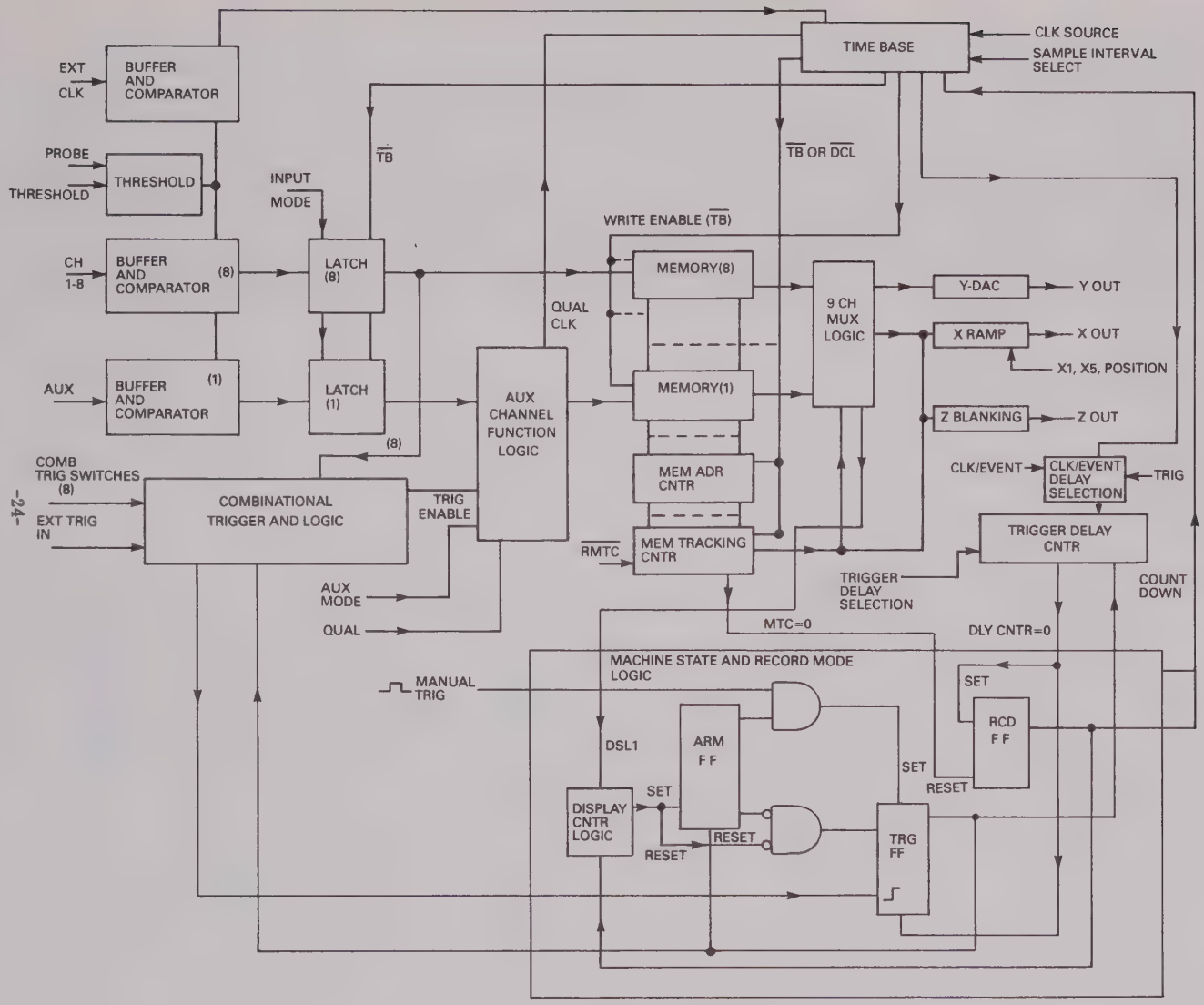


Figure 4.11 Auto Delay Trigger Record/Clock Delay and Event Delay

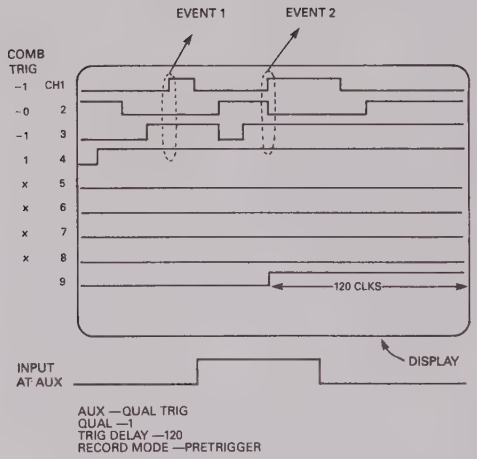


Figure 4.12 AUX and QUAL Conditions

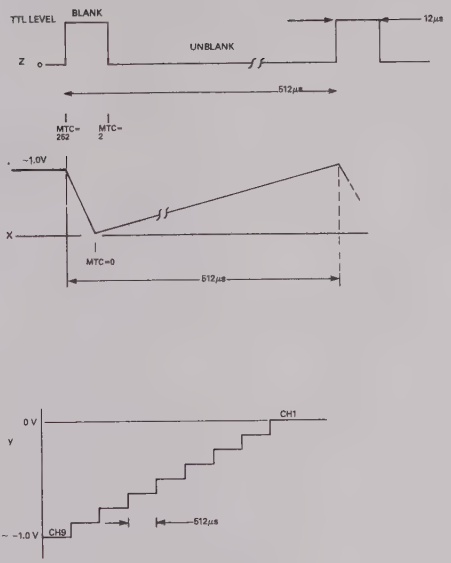


Figure 4.14 X, Y, Z Display Signals

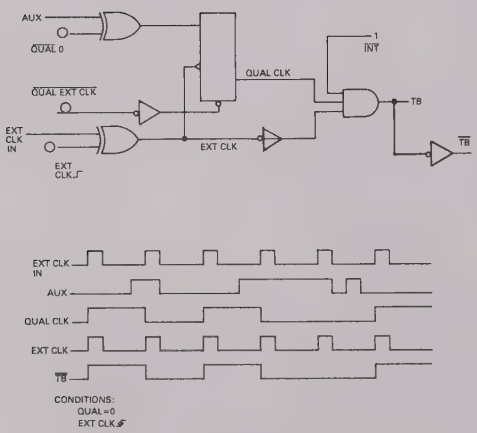


Figure 4.13 Typical EXT Clock Qualifying Waveforms

SECTION V

CALIBRATION PROCEDURE

5.1 Calibration of Display Output

Adjustments are provided to calibrate the "X" and "Y" outputs of the 920-D to a specific output device. If accurate time measurements are to be made, the 920-D and the display device must be calibrated as a system. Before leaving the factory, the "X" and "Y" outputs are set at 1.0 V p-p (X1) and 0.8 V p-p respectively. Figure 5.1 shows the location of the adjustments on the Main board for the "X" and "Y" levels.

Connect the 920-D to the display as shown in Figure 3.3.

Turn on both instruments and allow them to warm up for at least 5 minutes, then proceed as follows:

1. Remove the top cover of the 920-D and locate the Main board. This board is located on the bottom of the unit. The potentiometers are located near the Rear Panel on the Main board. The appropriate adjustments are easily made from the top. Place the 920-D into TTL X1 Threshold mode, and depress the MAN TRIG ARM then MAN TRIG switch.

2. Locate the potentiometer marked "Y". Adjust "Y" so that each of the nine lines in the display mode are centered on each of eight divisions of the scope face.

3. Ensure that 920-D expansion is X1 and that the scope expansion is also X1. Locate the potentiometer labeled "X". Adjust "X" to give full-scale display in the horizontal direction.

4. Adjust the character height to the desirable size by the potentiometer on the Main board located near the "X" and "Y" adjustments. Optimum height is achieved when the data on a channel is visibly separate from another channel.

The display adjustment is complete and the top cover may now be replaced on the 920-D.

5.2 Recalibration of Internal Circuits

The following calibration procedures are intended to be used in recalibrating the internal circuits of the 920-D. The entire instrument was calibrated before shipment and should not require any recalibration for at least six months or 1000 hours of operation.

5.3 Required Test Equipment

The following test equipment are required to calibrate the Model 920-D.

1. A digital voltmeter, DC range 0-20 V minimum, 4-1/2 digit resolution minimum.

2. An oscilloscope: 2 channel DC to 200 MHz input bandwidth. Horizontal resolution to 1 ns.*

3. A pulse generator capable of +5 V into 50 Ω.*

*NOTE: The equipment listed in Section 5.3 (numbers 2 and 3) are only required for Probe Compensation Adjustment (see Section 5.6).

5.4 Power Supply and Threshold Verification

Before recalibrating any circuit in the 920-D, it is necessary to check power supply outputs to ensure proper levels because the power supply is composed of monolithic regulators; if any supply is not within specification a part will be required for replacement. The thresholds are set by precise resistors (1%) so if any level does not meet specification a replacement part will be required. The verification is accomplished as follows:

1. Remove four screws from the side of the instrument.

2. Remove top cover.

3. Referring to Figure 5.1, Main board view, connect the voltmeter between the +5 TP and ground TP. Voltage should be 5.00 ± 0.25 VDC.

4. Connect voltmeter to -5.2 TP. Voltage should be -5.20 ± 0.25 VDC.

The above verification must be correct for further calibration. The thresholds are checked with the Front Panel TEST jack and switches. Connect voltmeter to the TEST jack and ground (BNC). Check levels as follows:

Threshold Control Position	Level at Test Jack			
TTL (X1)	1.40	±	0.07	VDC
ECL (X1)	-1.30	±	0.07	VDC
VAR (X1)	±2.85 min		±3.50	max
TTL (X10)	0.140	±	0.010	VDC
ECL (X10)	-0.130	±	0.010	VDC
VAR (X10)	±0.28 min		±0.35	max

5.5 Input Offset Adjustment

Offset adjustment is made to ensure proper operation of the input amplifiers. The E421 (FET) is selected for $I_{DSS} \leq 6$ mA. The adjustments are accomplished as follows:

1. Ground Threshold Test point (0 V).

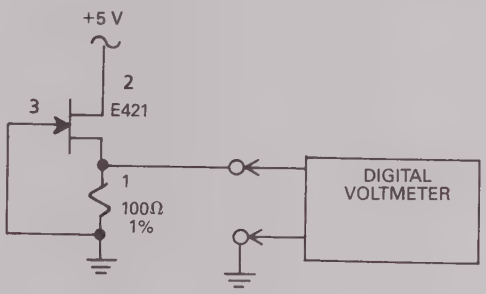
2. Using Figure 5.1, locate the area called Input Offset Adjust. Each amplifier has a feed-through that is used as the Offset TP (see Figure 5.1).

3. Locate Q11 (E421) and the Offset TP for Q11. Connect voltmeter between Offset TP and ground.

4. Adjust for 0.0 ± 0.5 mV DC. Repeat this step for Channels 1-8, AUX, and EXT CLK.

5. If offset cannot be obtained or failure occurs, replace E421 (FET) with a selected device.

NOTE: The parameter the E421 must pass is selected by the following circuit:



$V_s \leq 0.6$ V

To aid in finding all devices in each amplifier, use schematics and assembly drawings for Main board in Section VII.

5.6 Probe Compensation Adjustment

The Model 920-D has a PROBE COMPENSATION TEST point that allows a X10 probe to be monitored while the probe is compensated to the instrument's input amplifier characteristics. The adjustment is accomplished as follows:

1. Properly compensate a probe (resistive) to an oscilloscope (TEK 475 or equivalent). This probe and oscilloscope will monitor the adjustment for compensation of a probe.

2. Connect the monitoring probe to PROBE COMPENSATION TEST point on the Front Panel of the instrument.

3. Connect a probe to be compensated to Channel 1 BNC.

4. Adjust an external pulse generator for 1 kHz square wave at +5 V levels (0 V baseline). Input this signal to the probe under test (Channel 1).

5. Monitor oscilloscope for a signal, while adjusting the trim capacitor in the probe (Channel 1) for a good waveform.

6. Repeat steps 3-5 for the rest of the probes to be used with the Model 920-D.

The probes are now ready for use with the Logic Analyzer. A properly adjusted probe can be used in Channels 1-8, AUX, and EXT CLK.

THIS COMPLETES THE CALIBRATION OF THE MODEL 920-D LOGIC RECORDER.

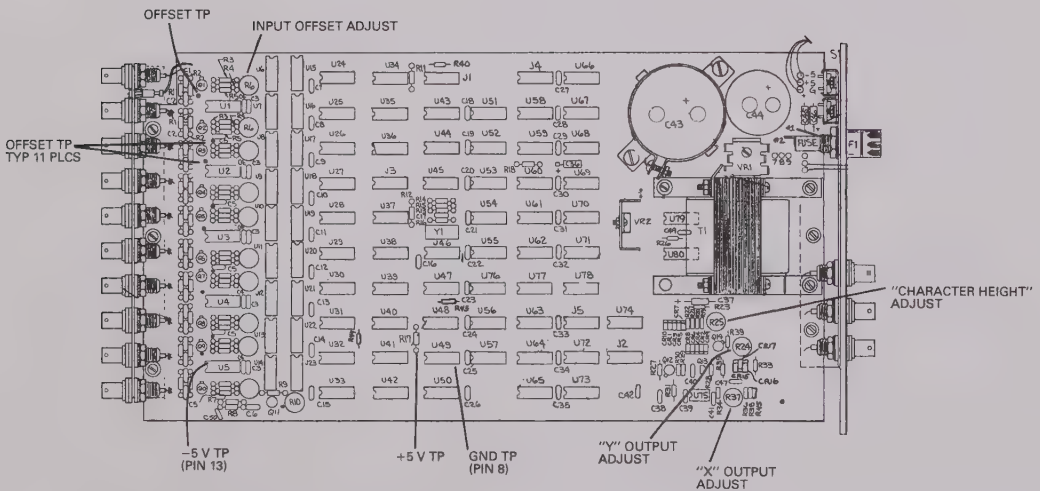


Figure 5.1 Location of Adjustments

SECTION VI

MAINTENANCE PROCEDURES

6.1 Introduction

This section covers maintenance and disassembly procedures for troubleshooting and repair of the Model 920-D. Repair is performed with the aid of a diagnostic procedure for the unit, a technical description, and schematic diagrams.

Waveform photographs have been included with the schematics to aid service personnel who wish to troubleshoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800 TWX (910) 338-0509.

In summary, there are two methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Troubleshoot the problem to the component level with the aid of the troubleshooting procedure and schematics or with the aid of factory personnel.

6.2 Required Test Equipment

The following test equipment is required to conduct the diagnostic procedure:

1. Two pulse generators capable of 1-ns rise and fall times. A minimum pulsewidth of 2 ns of output adjustable from -5 to +5 V into 50 Ω with single pulse capability.

2. An oscilloscope: Two channel DC to 200-MHz input bandwidth. Horizontal resolution to 1 ns.

3. Digital voltmeter: Range 0-20 V minimum, 4-1/2 digit resolution.

If a display device is not normally used with the Model 920-D, an additional oscilloscope or CRT display will be required during the test period. This latter oscilloscope need only have a 2-MHz input bandwidth.

6.3 Diagnostic and Troubleshooting Procedures

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
6.3.1 Equipment Set-up	
Connect a display device to the 920-D as per Figure 3.3. Turn on the 920-D and the display and allow them to warm up for a few minutes.	
NOTE: Display may not be present at this time.	
Set Front Panel controls as follows:	
Delay Source - Clock Delay Record Mode - Delay Man Delay - 000 Threshold - TTL (X1) Aux - Input Int Clk - 0.05 µs Sample Clock Source - Int Horizontal - X1 (Normal) Qualifier - 0 Combinational - X (CH 1) -X (CH 8)	
Press MAN ARM switch down. ARMED light should come on. Press MAN TRIGGER switch. Display should now show nine traces, and ARMED light should be extinguished.	ARM light not illuminated. Verify that test point 1 is TTL high level. No display. Verify that test point 2 is TTL low level. Verify that test point 6 is TTL high level. Observe waveform at test points 3, 4, and 5 (Z, Y and X).
Set Front Panel controls as follows: Record Mode - Delayed Auto	
Press MAN ARM switch down. ARMED light should come on. Press MAN TRIGGER switch. Display should show nine traces, and ARMED light should be illuminated.	No display. Verify above signal as for Delay Man. ARMED light not illuminated. Verify that test point 7 is logic high level. Observe waveform at test point 8(IC U53) is as in photograph.
Set Front Panel controls as follows: Record Mode - Pretrigger	
Press MAN ARM switch down. ARMED light should come on. Record light should come on, and display should be BLANKED. Press MAN TRIGGER switch. Display should show nine traces; the two lights should be extinguished.	Display not blanked. Verify logic low level at test point 9 after MAN ARM, and test point 2 is logic high level. No display. Test point 10 will be logic high to low as MAN TRIG is depressed (one time event). Test point 2 should be logic low level.

DIAGNOSTIC PROCEDURE

6.3.2 Combinational Trigger and Data Input

Set Front Panel controls as in step 6.3.1, except Record mode to Delayed Auto. Set an external pulse generator for 1 µs square wave at +3 VDC level (0 VDC baseline). Input the signal to Channel 1, and place Channel 1 to "1" combinational . Verify response as in Figure 6.1. Place Channel 1 to "0". Verify response as in Figure 6.2. Return Channel 1 to "X". Repeat above procedure for Channels 2 through 8. Place external signal into AUX BNC, manually arm, and then trigger. Observe signal on the ninth trace of the display. Verify INT CLK performance using Table 6.1 with Channel 1 to set to "1" and all others to "X".

Table 6.1

INT CLK Settings (µs)	Input	Response (Figure No.)
0.05	13.5 µs*	6.3
0.10		6.4
0.20		6.5
0.50	135 µs*	6.3
1.00		6.4
2.00		6.5
5.00	135 ms*	6.3
10.00		6.4
20.00	*Period of	6.5
50.00	Waveform (square wave)	6.6

Place TRIG OUT (+) from pulse generator into TRIG IN on 920-D with signal in Table 6.1 inputted, and Channel 1 set to "X". Instrument should still trigger and display. Remove TRIG IN signal, and place Channel 1 to "1". Using the first test set up in Table 6.1, observe TRIG OUT on the rear panel of 920-D with an oscilloscope. Signal should be 13.5 µs (period) at Transistor-Transistor levels. Place AUX to QUAL TRIG, and observe that TRIG OUT remains the same. Place QUAL to 1. The scope should show Transistor-Transistor High level. Return QUAL to 0. Place Channel 1 to

TROUBLESHOOTING PROCEDURE

Display not as in Figure 6.1.
Verify test point 11 is inputted signal with the INT CLK sampled edges (jitter). Test point 12 is high level, and test point 13 is high level.

Display not as in Figure 6.2.
Verify same signal as for Figure 6.1 test. Test point 13 is high level, and test point 12 is low level.

Failure of any response of Table 6.1. Verify test point 14 is waveform of INT CLK selected.

No trigger and display.
Verify test point 15 is TRIG OUT (+) signal. Test point 11 is TRIG OUT (+) only jittered on the edges.

TRIG OUT not correct.
(a) Signal not present: Verify test point 11 is input signal.
(b) Not high level: test points 17 and 18 high level.

DIAGNOSTIC PROCEDURE

"1" with signal (13.5 μs) inputted. Change INT CLK to 0.5 μs. Pull HORIZONTAL EXPANSION (X5) outward. Display should look as in Figure 6.7. Adjust HORIZONTAL POSITION knob to right and left to verify that all data can be observed. Return EXPAND switch to in position, and Channel 1 to "0".

6.3.3 Delay Verification

CLOCK DELAY

Place 920-D Front Panel controls as in Step 6.3.1, except Record mode to Pretrigger and AUX to QUAL TRIG. Place INT CLK to 0.50 μs and Channel 8 to "0". Input 13.5 μs signal to Channel 8. MAN ARM instrument and increase DELAY (0-9 in each digit location). The 920-D needs to be manually armed each time DELAY is increased. The display should move in equal increments, and Channel 9 should show an edge moving across display as DELAY is increased until 030 (high level shown).

Set Front Panel controls as follows:

Record Mode - Delayed Man

Repeat above procedure for Delayed Man. Channel 9 should remain low level (no signal). Verify response. Change Delayed Man Record to Delayed Auto, and verify delays (0-9 in each digit location) as for Delay Man, but manually arming instrument is not required.

EVENT DELAY

Set Front Panel controls as follows:

Record Mode	-	Pretrigger
Delay Source	-	Event Delay
Delay	-	001
Combinational	-	X(CH 1) - X(CH 7), 1 (CH 8)
Int Clk	-	0.5 μs
Aux	-	Qual Trig

Input to Channel 8 the external signal (13.5 μs square wave). Manually arm the in-

TROUBLESHOOTING PROCEDURE

Display not as in Figure 6.7.
Observe waveform at test point 5 (IC U75) is as in photograph. Test point 19 is +5 V.

Display movement incorrect.
Verify proper data bits at test points 21-32 for digits loaded (straight BCD). Test point 33 is logic high level.

Channel 9 data incorrect.
Observe test point 34 is logic high level.

Display movement incorrect.
Verify test points 35 and 36 are logic high level.

Auto-Delay not proper.
Observe test point 1 is high then low signal. Delay=000, observe test point 37 as in photograph (Delay increase 1 cm/digit). Delay=010, observe test point 37 as in photograph.

Display not as in Figure 6.8.
Verify test points 38, 39 and 41 are high levels. Observe input waveform at test point 40.

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
strument. Observe display as in Figure 6.8. Place DELAY to 004, and manually arm. Observe that waveform on Channel 9 is windowed about five positive transitions (Figure 6.8 shows two transitions.)	
Set Front Panel controls as follows: Record Mode - Delayed Man Delay - 000 Combinational - X(CH 1) - X(CH 8).	
Use the same Front Panel controls as for above procedure (Event Delay), except where noted. Input the 13.5 µs square wave signal to Channel 8. Place Channel 1 to "1", and input a second pulse generator with single pulse output (Manual). Set pulsewidth for 50 µs. Set DELAY to 002. Manually arm instrument. Observe display while manually pulsing generator. Display should be as in Figure 6.9 after three pulses. Increment DELAY to 009. Manually arm instrument. Pulse the generator ten times, and observe display shifts (data). Remove external signals.	Display not as in Figure 6.9. Verify proper number loaded into test points 21-32 (straight BCD). Test point 36 is high level. Test point 35 is high level.
6.3.4 High-Speed Performance Check	
Set Front Panel controls as in step 6.3.1, except INT CLK to 0.05 µs Latch. Set Record mode to Delayed Auto, and Combinational to all "Xs". Use the signals as called out in Table 6.2 to verify input performance of all Channels. After channel is checked "1" and "0" positions, return combination to "X". The display should show no data drop outs in all checks.	
Use a X10 resistive probe to check the X10 threshold responses. Use Table 6.2 values to verify performance with X10 TTL and X10 ECL thresholds (switch on Front Panel), in place of the X1. Signals should be set up at probe tip input. Remove external signals.	Failure of X10 performance. Verify X10 threshold at test point on front panel.
Set Front Panel controls as follows: Int Clk - 0.05 µs Sample Combinational - X(CH 1) - X(CH 7), 1 (CH 8) Threshold - TTL (X1) Record Mode - Delayed Auto	

DIAGNOSTIC PROCEDURE

Table 6.2
Verification of Input Performance

Mode	Pulse-Width (ns)	Period (ns)	Signal Level (V)	Over-drive (mV)
X1 TTL Latch	10 (at +1.4 V)	200	0 to +2 (0 REF) +3 to 1 (+3 REF)	300
Sample	60 (at +1.4 V)	500	0 to +2 (0 REF) +3 to 1 (+3 REF)	
X1 ECL Latch	10 (at -1.3 V)	200	-1.8 to -0.8 (-1.8 REF) -0.8 to -1.8 (-0.8 REF)	
Sample	60 (at -1.3 V)	500	-1.8 to -0.8 (-1.8 REF) -0.8 to -1.8 (-0.8 REF)	

Use Front Panel control settings as called out in step 6.3.1, except where noted above. Input to Channel 8 a 13.5 µs square wave at +3 V amplitude (0 V baseline). Set an external generator for a 20 MHz signal into EXT CLOCK. Observe display for waveform, and place Clock Source to EXT ⎍. Note no change in display. Change source to EXT ⎎. No change in waveform; place QUAL to 1. Display movement stopped; return QUAL to 0 and Clock Source to INT.

THIS COMPLETES THE DIAGNOSTIC PROCEDURE FOR THE MODEL 920-D.

TROUBLESHOOTING PROCEDURE

Failure of value in Table 6.2. Verify test point 41 for input signal (CH 1 failure). Check signal in failed channel path. Latch test: test point 41 is logic High. Sample test: test point 41 is logic Low.

Verify change of display. Test point 42 is 20 MHz Clock.

Display not stopped. Verify test point 42 is logic High level, and test point 43 is logic Low level.

6.4 Disassembly Procedure

The following are disassembly procedures for the Model 920-D Front Panel and Main board subassemblies. See Figure 6.10, Disassembly Views.

6.4.1 Main Board

Disconnect power cord.
Remove top cover screws (4 screws).
Remove top cover by gently pulling outward on plastic cover, and lifting cover upward.
Place bail assembly away from instrument.
Remove the eight screws on the Main board as shown in Disassembly View.

The Main board is now ready for service. The front and rear panels are attached to the Main board to make an electrically testable subassembly. For reassembly, reverse the above procedure.

6.4.2 Front Panel Subassembly

If it is necessary to disassemble the Front Panel to replace a component, proceed as follows:

Remove the Main board from case as in 6.4.1 procedure. The Front Panel subassembly is now ready for service. Remove all ribbon cables to Main board and AC power connector (TO POWER ON SWITCH).

Digitswitch Board:

Remove the three screws (two in corners and one in lower center).
The Digitswitch board can now be removed from Front Panel board.

Front Panel Board:

Remove the two holddown screws (TO MAIN BOARD) as shown in Figure 6.10, Disassembly Views. The Front Panel subassembly is now separate from Main board. Remove Digitswitch board as above. Use a plier to gently remove the three standoffs (Digitswitch board support). Use a 0.050-inch Allen head driver to remove the two screws in the HORIZONTAL POSITION knob. Remove knob from Front Panel. Remove the two screws in lower right and left edges of the Front Panel board assembly.

NOTE: The black masks (around switches) are fitted to each switch, so if total disassembly is required make sure proper mask is with each switch.

Pull Front Panel Decorative and Front Panel board slowly apart.

The Front Panel board is totally serviceable now. To reassemble, reverse the above procedure starting with Front Panel board.

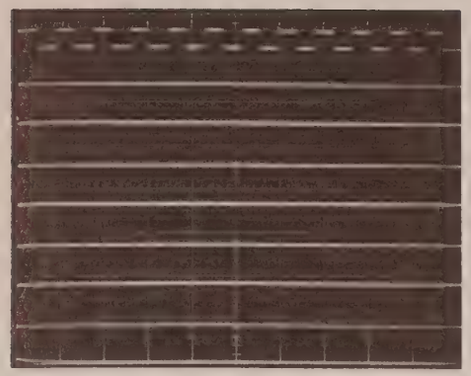


Figure 6.1

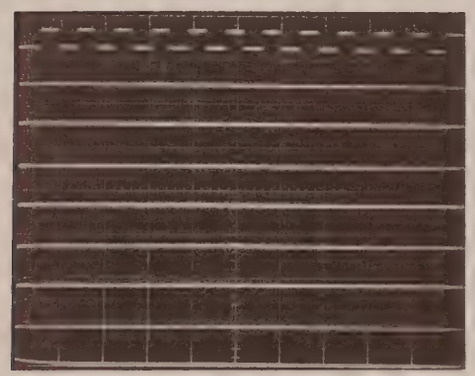


Figure 6.2

Figure 6.3

Figure 6.4

Figure 6.5

Figure 6.6

Figure 6.7

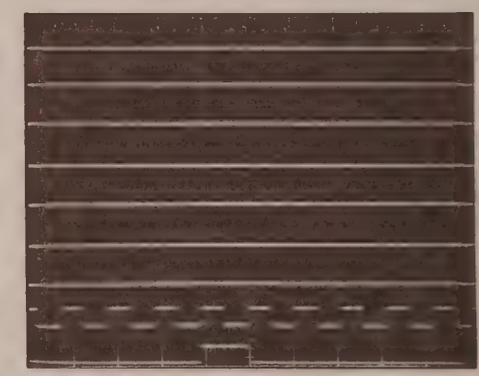


Figure 6.8

Figure 6.9

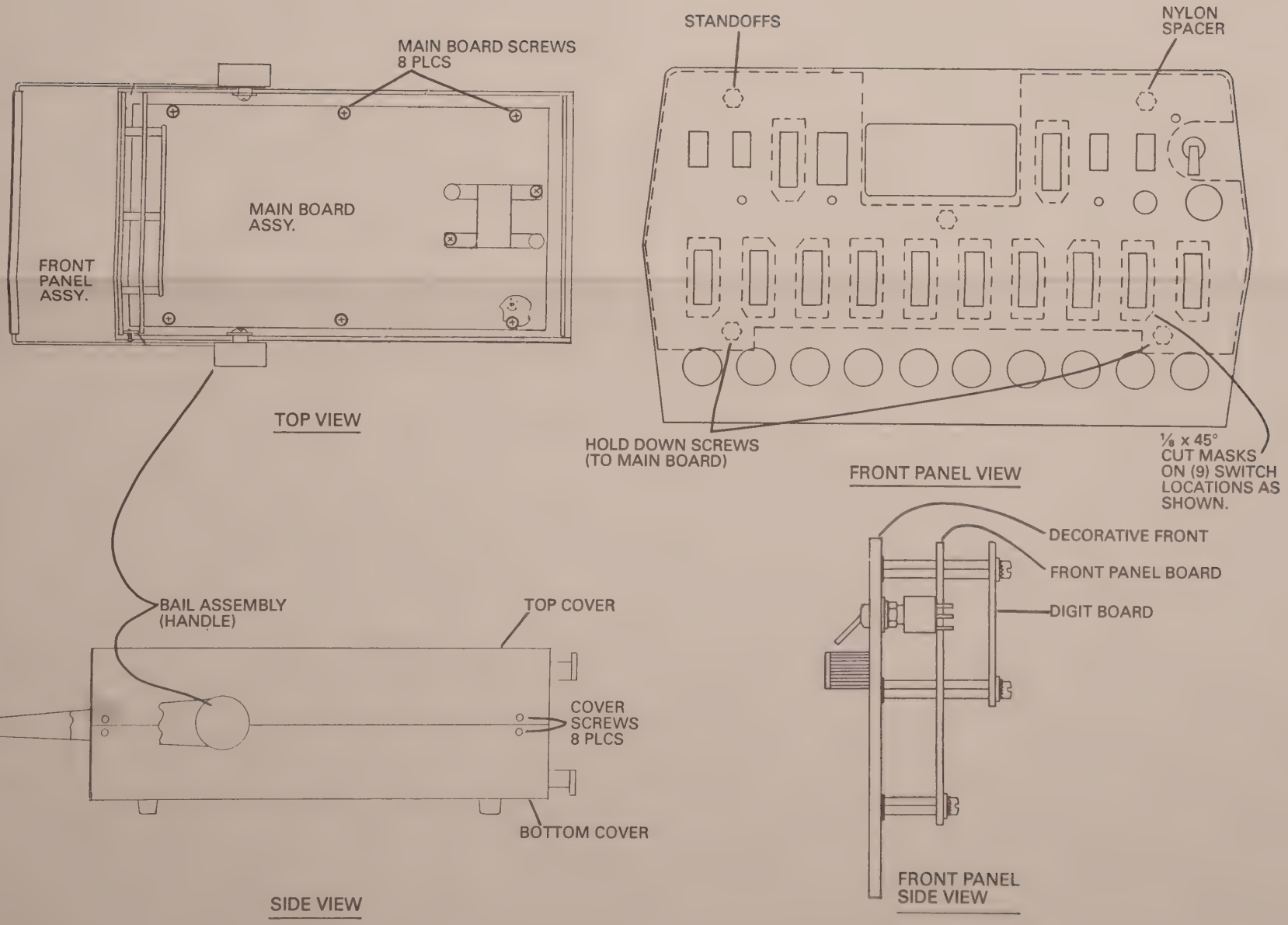


Figure 6.10 Disassembly Views

SECTION VII

SCHEMATICS AND ASSEMBLY DRAWINGS

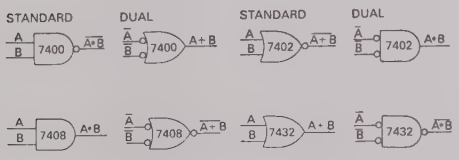
7.1 Introduction

This section contains the schematics and assembly drawings for the Model 920-D. Test points and waveform photographs are included, along with troubleshooting aids.

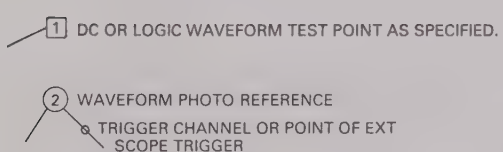
7.2 Logic Symbols and Reference Designators

LOGIC SYMBOLS

The Logic Symbols used in this manual depict the logic function performed and may be different than those published in the manufacturers' data book.



REFERENCE DESIGNATORS



7.3 Definitions of Troubleshooting Aids

The Model 920-D schematics have troubleshooting aids on them. The aids are designed to help the user understand the functions of the circuits in the different modes.

7.3.1 Mnemonics and Abbreviations - Definitions

PRETG - Pretrigger Mode

STRTS - Starts

RCD - Record

DLY - Delay (Mode)

CNT - Count

TRIG - Trigger

F/F - Flip-Flop

DIP - Display

AUTO - Automatic

MAN - Manual

MEM - Memory

CH - Channel

MTC - Memory Tracking Counter

CLK - Clock

POS - Position

ADD - Address

EN - Enable

COMP - Components

DWN - Down

7.4 List of Drawings

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Figure 7.2	Front Panel Assembly	41
Figure 7.3	Digitswitch Assembly	42
Figure 7.4	Front Panel Schematic	43
Figure 7.5	Main Board Assembly	44
Figure 7.6	Waveform Photographs	45
Figure 7.7	Main Board Schematic	47
Figure 7.8	Power Supply Schematic	49

7.5 Parts Lists

The materials in the following lists are subject to change without Gould Inc.'s prior notification. For list verification, contact the Customer Service Department at the factory: Phone (408) 988-6800 TWX (910) 338-0509.

7.5.1 List of Parts Lists

	Page
Top Assembly	50
Front Panel Assembly	51
Front Panel Board, Assembly	52
Digitswitch Board, Assembly	53
Main Board	54
Bail Assembly	58

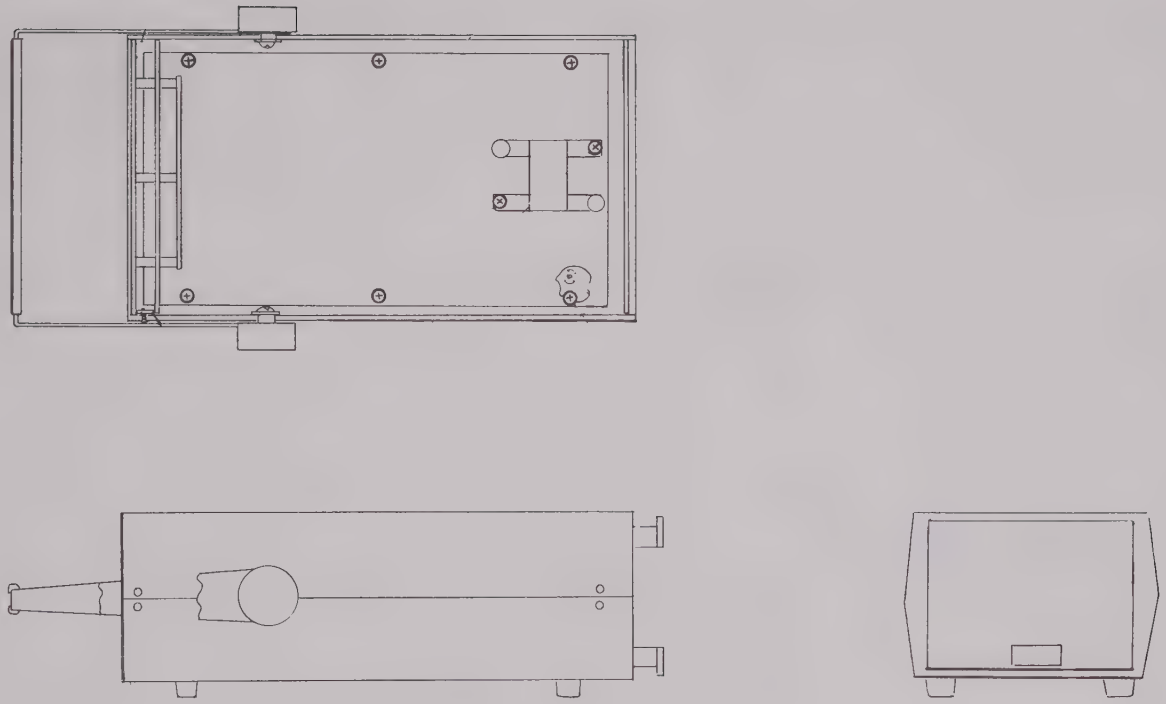
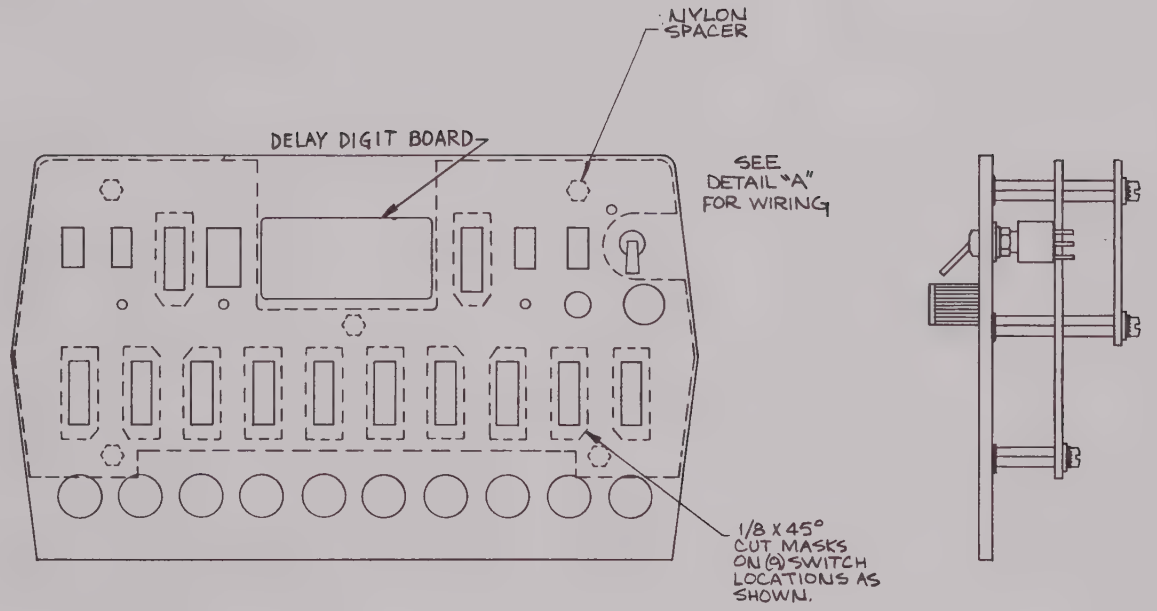
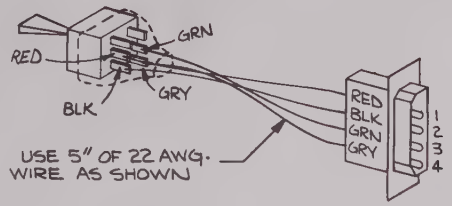


Figure 7.1 Top Assembly





DETAIL "A"

Figure 7.2 Front Panel Assembly

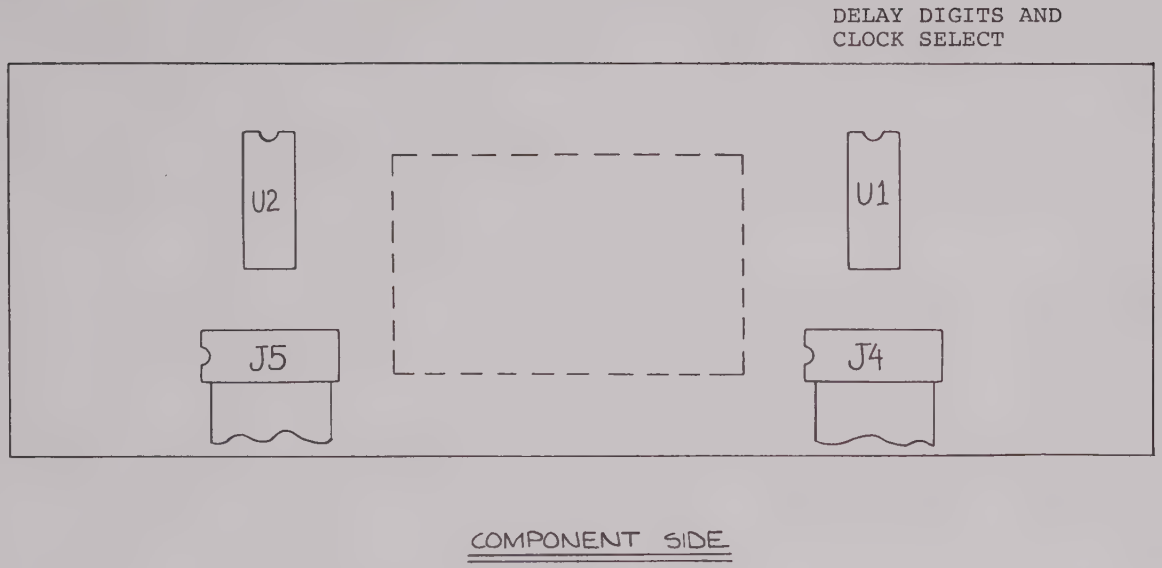


Figure 7.3 Digitswitch Assembly

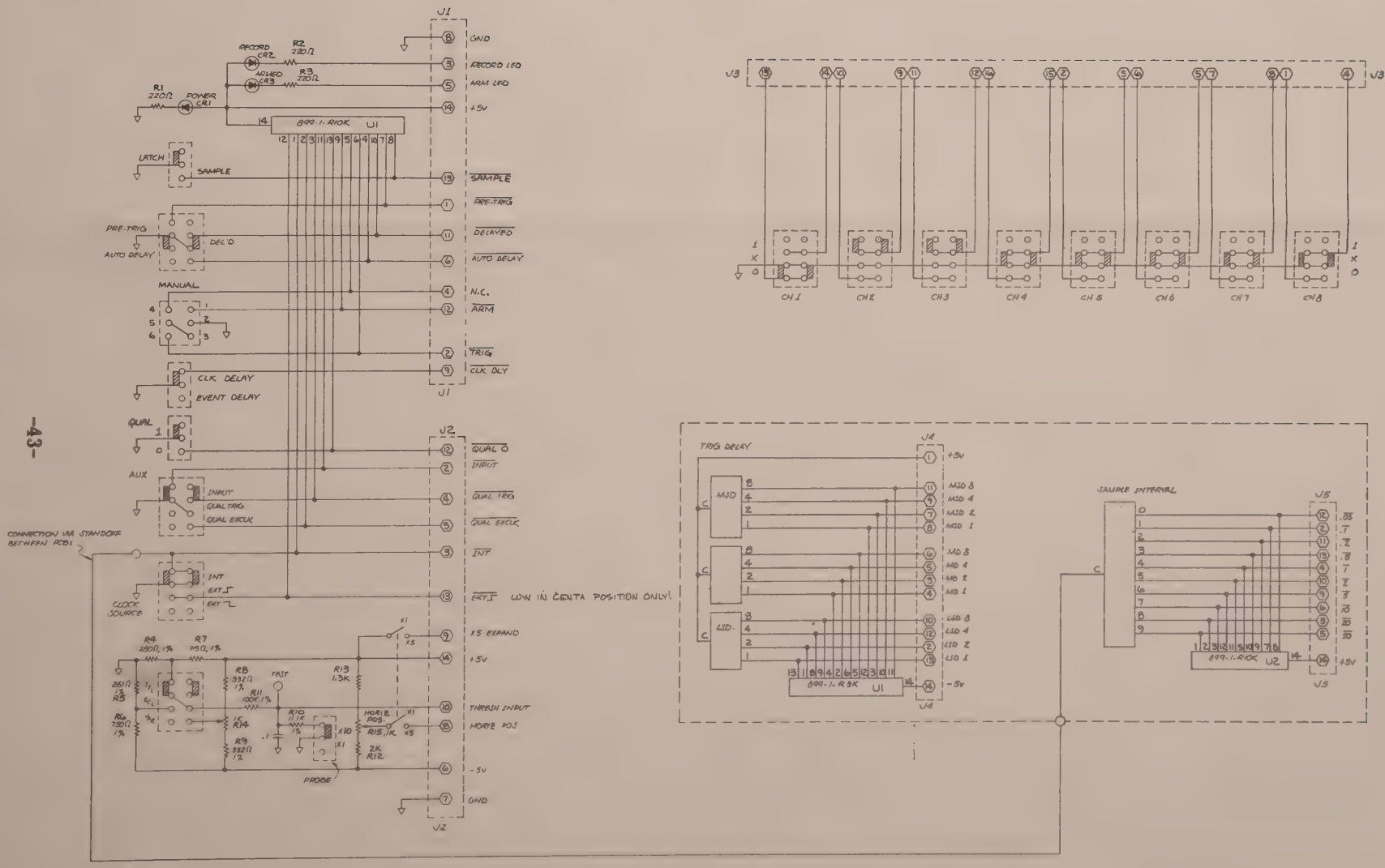


Figure 7.4 Front Panel Schematic

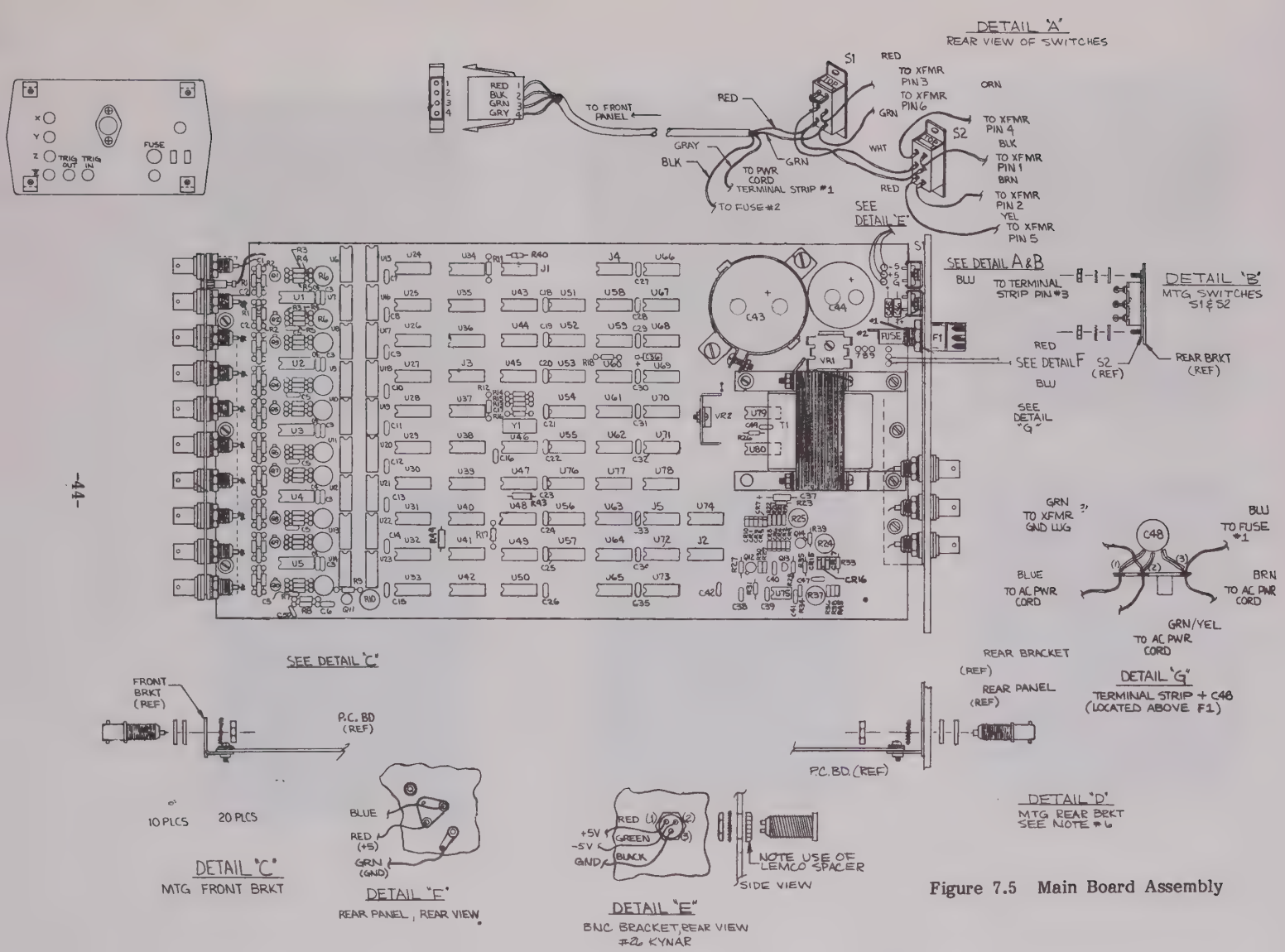
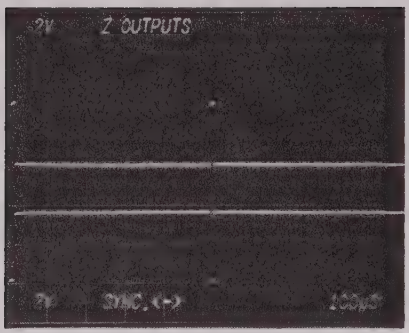
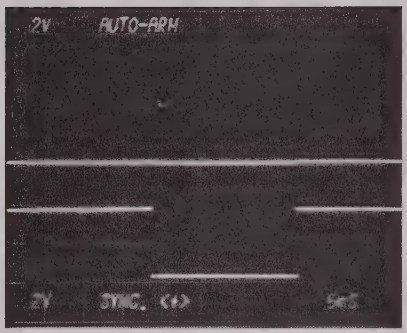


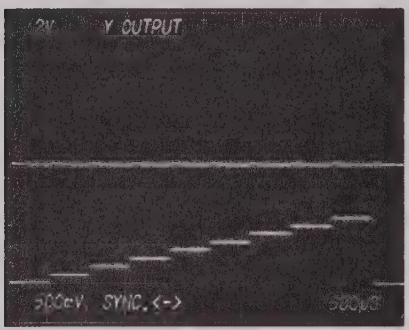
Figure 7.5 Main Board Assembly



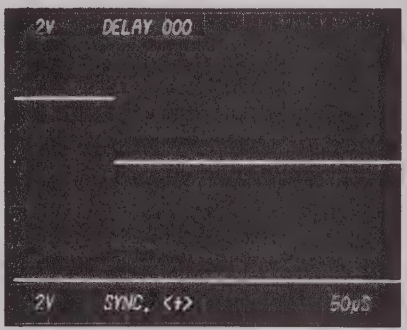
1. Test Point 3



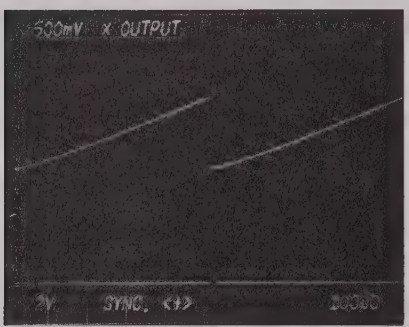
4. Test Point 8



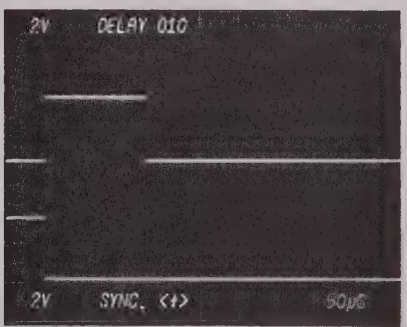
2. Test Point 4



5. Test Point 37

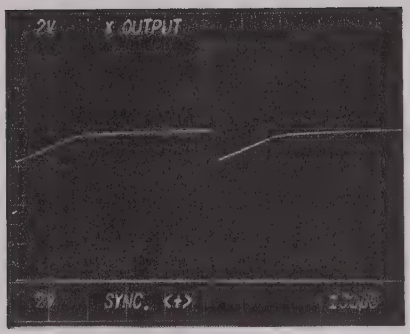


3. Test Point 5



6. Test Point 37

Figure 7.6 Waveform Photographs



7. Test Point 5

Figure 7.6 Cont. Waveform Photographs

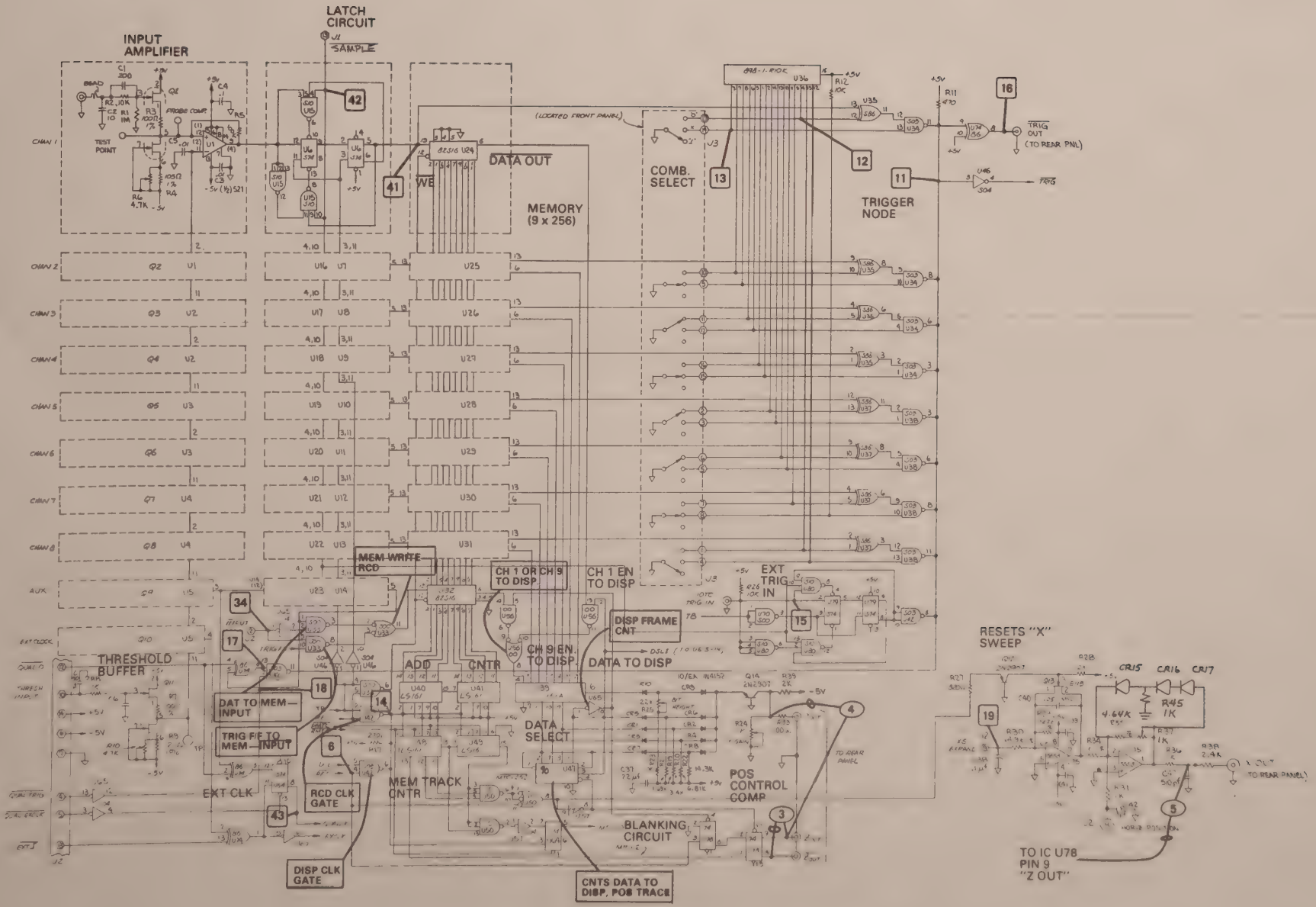


Figure 7.7 Main Board Schematic

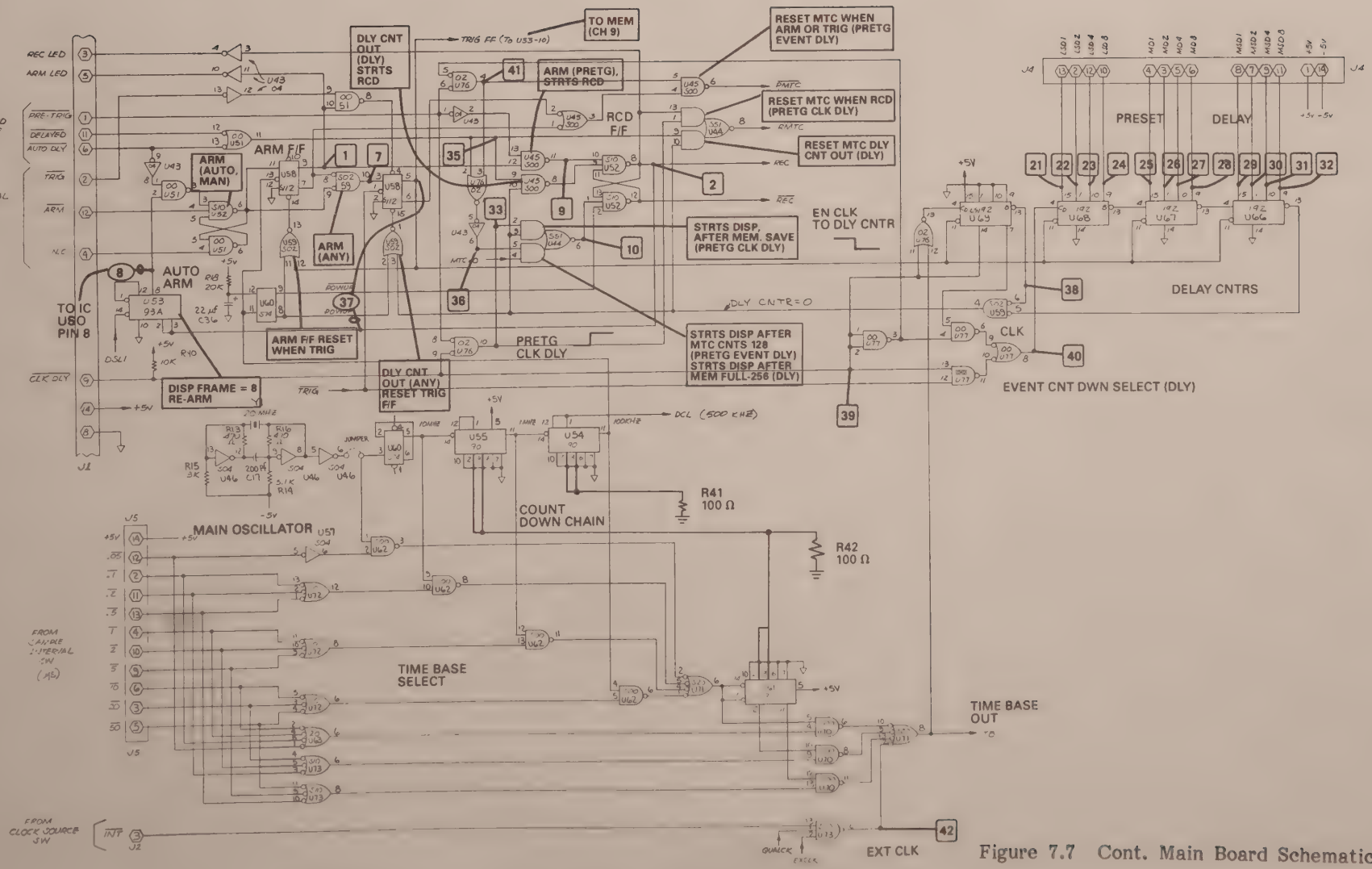


Figure 7.7 Cont. Main Board Schematic

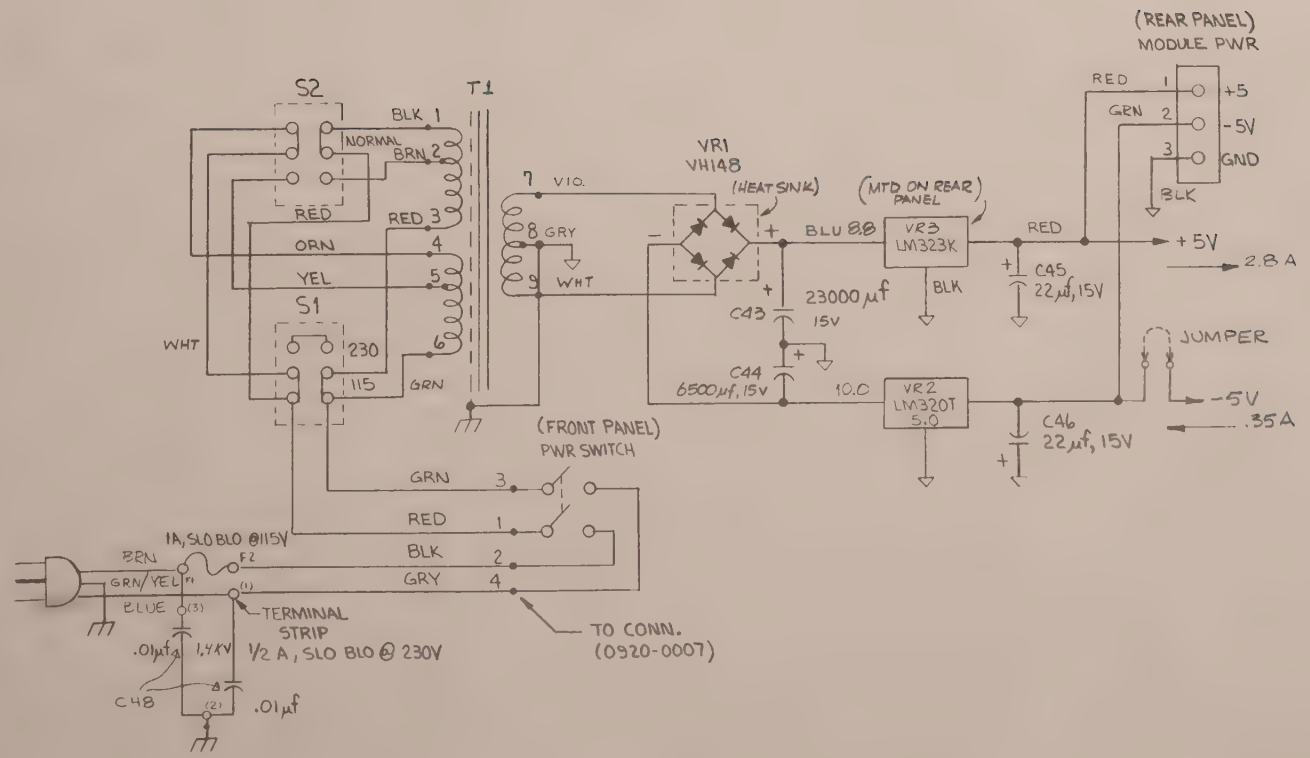


Figure 7.8 Power Supply Schematic

Top Assembly

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0920-0020	CASE				
2						1	0920-0019	FRONT FACE PLATE			ASSY	L/M
3						1	0920-0005	MAIN BD			ASSY	L/N
4						1	0920-0026	BOTTOM				
5						1	0920-0033	BAIL ASSY				L/M
6												
7						4	0920-0038	FASTENER, BRACKET				
8						8	———	SCREW		ALLANDER	FLAT HD #6-32 x 3/8 LG	
9						1	0610-0032	SERIAL TAG				
10						4	7000-0278	RUBBER FEET				
12						8	—	SCREW			#6 x 3/8, PAN HD	
13						8	—	LOCK-WASHER			#6	
14						8	—	FLAT, WASHER			#6	
15						8	7000-0279	ONSERT			#6	
16						4	7000-0280	ONSERT			#8	
17						4	—	SCREW			#8-32 x 5/8 PAN HEAD	
18						4	—	LOCK-WASHER			#8	

Front Panel Assembly

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0920-0014	FRONT PANEL				
2						1	0920-0010	FT. PNL BD ASSY				L M
3						1	0920-0015	DIGGI-BD ASSY				L M
4						12	0852-0066	SWITCH MASK				
5						1	6000-0024	CONNECTOR				
6						1	6500-0016	KNOB				
7						1	6600-0019	PWR SWITCH				
8						4	6100-0005	PINS-MALE		AMP 1-480426-0		
9						3	7000-0199	STANDOFF		SMITH # 8235	6-32 x 5/8 FEMALE/MALE	
10						4	7000-0260	STANDOFF		SMITH # 2323	6-32 x 3/4 HEX	
11						5	—	SCREW, PAN HD			#6-32 x 5/16	
12						5	—	WASHER, LOCK			#6	
13						11	—	WASHER, FLAT			#6	
14						1	7000-0284	STANDOFF		AMATOM 8218-N 0632	6-32 x 3/4 HEX, NYLON	
15												
16												
17												
18												

Front Panel Board, Assembly

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0920-0012	FR. PANEL BD.				
2						3	3000-2200	RESISTOR	R1-3		220Ω, ¼W, 5%	
3						1	3100-2800	"	R4		280Ω, ⅛W, 1%	
4						1	3000-1301	"	R13		1.3K, ¼W, 5%	
5						1	3100-2610	"	R5		261Ω, ⅛W, 1%	
6						2	3100-3320	"	R8,9		332Ω " "	
7						1	3100-7150	"	R7		715Ω " "	
8						1	3100-7500	"	R6		750Ω " "	
9						1	3100-1102	"	R10		11.0K " "	
10						1	3100-1003	RESISTOR	R11		100K, ⅛W, 1%	
11						1	3500-1010	RES, VARIABLE	R14	A-B TYPE W	1K, ⅜ SHAFT	
12						1	3700-0001	RES. PACK	U1	899-1-R10K	10K	
13						1	4000-0025	CAPACITOR	C1		.1μF	
14						1	6000-0041	TEST JACK			BLK	
15						3	6100-0069	L.E.D. SOCKET				
16						2	6400-0040	DIODE	CR2, CR3	HP 5082-4584	YELLOW	
17						1	6600-0068	SW1, TOGGLE		C+K 7215-J2-V30	DBL MOMENTARY (ON) ON (ON)	
18						12	6700-0008	SW1, SLIDE		CW G-328 BUTTON G-02-68	3 POS, 2 POLE PINS G-20-42	
19						4	6700-0012	SW1, SLIDE		CW G-326 BUTTON G-02-68	2 POS, 2 POLE - EARS PINS G-20-42 REMOVED	
20						1	7000-0136	STANDOFF			8-32 x ¾ HEX SWAGE TYPE	
21						1	0920-0037-10	CABLE ASSY	J3		16 PIN	
22						1	0920-0037-20	CABLE ASSY	J1		14 PIN	
23						1	0920-0037-40	CABLE ASSY	J2		14 PIN	
24						1	3000-2001	RESISTOR	R12		2K, ¼W, 5%	
25						1	3500-1024	RES, VARIABLE	R15	A+B (ELMAR) 16M-682		
26						1	6400-0039	DIODE	CR1	HP 5082-4684	RED	
27												
28												
29												
30												
31												
32												
33												
34												
35												
36												

Digitswitch Board, Assembly

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0920-0017	FR. PANEL BD				
2						1	0920-0042	DIGITSWITCH		DIGITRAN 2900-B-95		
3						1	0920-0037-20	CABLE ASSY	J4			
4						1	0920-0037-30	CABLE ASSY	J5			
5						1	3700-0001	RES, FLAT PAK	U2	BECKMAN 899-1-R10K	10K	
6						1	3700-0024	RES, FLAT PAK	U1	BECKMAN 899-1-R3K	OR (ALLEN #314A-BRADLEY 3000Ω) 3K	
7												
8												

Main Board

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0920-0007	PWB				
2						1	3700-0002	RES PACK	U36	BECKMAN 898-1-R10K	10K 16 PIN RES PACK	
3						4	6100-0014	SOCKET	J1, J2, J4, J5	CIRCUIT ASSY CA-145-105D	14 PIN SOCKET	
4						1	6100-0009	SOCKET	J3	AMP/ BARNES 821-25011-164	16 PIN SOCKET	
5						10	2100-0001	FERRITE BEAD	CH1-9, EXT. CLK INPUT LEAD			
6						1	1800-0023	I.C.	U78	7474		
7						5	1700-0026	I.C.	U1-U5	521		
8						12	1800-0054	↑	U6-U14, U60, 64, 79	74S74		
9						12	1800-0060		U15-U23, 52, 73, 80	74S10		
10						9	1800-0081		U24-U32	82S16		
11						4	1800-0031		U33, U45, U62, U70	74S00		
12						3	1800-0059		U34, U38, U42	74S03		
13						2	1800-0206		U35, U37	74S86		
14						1	1800-0082		U39	74151		
15						4	1800-0125		U40, U41, U48, U49	74LS161		
16						2	1800-0005		U43, U65	7404		
17						1	1800-0136	↓	U44	74S51		
18						2	1800-0092	I.C.	U46, U57	74S04		
19						2	1800-0021	I.C.	U47, U53	7493A		
20						3	1800-0001	↑	U51, U56, U77	7400		
21						3	1800-0019		U54, U55, U61	7490A		
22						2	1800-0006		U72, U50	7410		
23						1	1800-0039		U58	74S112		
24						1	1800-0226		U59	74S02		
25						2	1800-0038		U63, U71	74S20		
26						3	1800-0041		U66-U68	74192		
27						1	1800-0018	↓	U74	7486		
28						1	1700-0018	I.C.	U75	5558		
29						1	1800-0003	I.C.	U76	7402		
30						1	1800-0122	I.C.	U69	74LS192		
31						1	4100-0044	CAP.,	C97		510pf, 500V, 5%	
32						11	4100-0008	CAP.,	(CHN 1-9 + CLK) C1, C17		200pF, 500V, 5%	
33						10	4100-0005	↑	(CHN 1-9 + CLK) C2		10pf, 500V, 5%	
34						38	4000-0005		(CHN 1, 3, 5, 7 + CLK) C3, 5, C7-15, C18-35, C49		.01 uf, 100V	
35						1	4000-0006	↓	C48		DUAL .01 uF 1.4 KV	
36						1	4200-0012	CAP.,	C40		.05, 100V 10%	

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37						12	4000-0016	CAP.,	C16, C38-39, 41, 42 (CHN1, 3, 5, 7 CLK) C4, C6, C50		.1 uf, 50V	
38						1	4400-0021	↑	C43	CGS233U015DDI	23000 UF, 15V	
39						1	4400-0010	↓	C44	CORNELL FAN6500-15-A1	6,500, 15V	
40						4	4300-0009	CAP.,	C36, 37, 45, 46		22 uF, 15V TANT.	
41						1	3100-6811	RES.,	R20		6.81 K, $\frac{1}{8}$ W, 1%	
42						1	3100-1432	RES.,	R22		14.3 K, $\frac{1}{8}$ W, 1%	
43						1	3100-1691	RES.,	R21		1.69 K, $\frac{1}{8}$ W, 1%	
44						10	3000-1004	RES.,	(CHN1-9 + CLK) R1		1M, 1/4W, 5%	
45						14	3000-1002	↑	(CHN1-9 + CLK) R2, R12, 23, 26, 40		10K, 1/4W, 5%	
46						11	3100-1000		(CHN1-9 + CLK) R3, R7		100Ω, 1/8W, 1%	
47						10	3100-1050		(CHN1-9 + CLK) R4,		105Ω, 1/8W, 1%	
48						10	3000-1003	↓	(CHN1-9 + CLK) R5,		100K, 1/4W, 5%	
49						11	3300-0064	RES., POT	(CHN1-9 + CLK) R6, R10	STERLING ELEC E086BD4K7W	4.7K, ± 20%	
50						3	3000-4700	RES.,	R11, 13, 16		470Ω, 1/4W, 5%	
51						1	3000-5101	↑	R14		5.1K, 1/4W, 5%	
52						1	3000-3001		R15		3K, 1/4W, 5%	
53						1	3000-2002	↓	R18		20K, 1/4W, 5%	
54						1	3100-3401	RES.,	R19		3.4K, 1/8W, 1%	
55						1	3000-8200	RES.,	R27		820Ω, 1/4W, 5%	
56						2	3000-2001	↑	R28, R39		2K, 1/4W, 5%	
57						1	3100-2493		R29		249K, 1/8W, 1%	
58						1	3100-6492		R30		64.9K, 1/8W, 1%	
59						1	3000-1000		R33		100Ω, 1/4W, 5%	
60						1	3000-2700		R17		270Ω, 1/4W, 5%	
61						1	3100-1001		R34		1K, 1/8W, 1%	
62						1	3100-4021	↓	R35		4.02K, 1/8W, 1%	
63						3	3000-1001	RES.,	R31, 36, R8		1K, 1/4W, 5%	
64						1	3300-0062	RES., POT	R24	STERLING ELEC E086BD1KW	1K, ± 20%	
65						1	3300-0065	RES., POT	R25	STERLING ELEC E086BD22KW	22K, ± 20%	
66						1	3300-0063	RES.. POT	R37	STERLING ELEC E086BD2K2W	2.2K, ± 20%	
67						1	3000-2401	RES.	R38		2.4K, 1/4W, 5%	
68						1	3100-1210	RESISTOR	R9		121Ω, 1/8W, 1%	
69												
70						10	1000-0002	DIODE	CR1-10	IN4152		
71						1	1200-0025	RECTIFIER	VR1	VARO VH148	6 AMP	
72												

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
73						11	0920-0025	JFET	Q1-Q11		E421 (SPECIAL SORT)	
74						2	1400-0001	TRANSISTOR	Q12, Q14		2N2907	
75						1	1500-0008	JFET	Q13		E113	
76						1	1700-0049	REGULATOR	VR2		LM320T	
77						1	7300-0013	FUSEHOLDER	F1			
78						1	0920-0024	TRANSFORMER	T1			
79						1	5100-0002	CRYSTAL	Y1		20 MHZ	
80						1	7000-0046	CAP., CLAMP	SANGAMO TYPE DCM	SANGAMO 115058-05	FOR C43	
81						1	7000-0265	HEATSINK		THERMALLOY 6030 D	NICKEL PLATED FOR VR2 (LM320T)	
82						1	7000-0032	HEATSINK		IERC PA2-1CB	FOR VR1	
83						1	6700-0015	SWITCH	S1, S2	C-W 6F 626 DPDT	G02-153	
84						1	0920-0022	REAR PANEL				
85						1	0920-0021	FRONT BRACKET				
86						1	0920-0023	REAR BRACKET				
87						1	6100-0103	SOCKET, PWR XSISTOR		CINCH 2TS3	CONNECTION TO 323	
88						16	6000-0003	BNC		KING	KC-79-46 (LONG BASE)	
89						32		BNC WASHERS			BNC-FLAT WASHER .500 O.D. x .062 THK	
90												
91						4	6100-0006	CONN PINS			FEMALE	
92						1	6000-0023	CONN 4 PINS				
93						A/R		SLEEVING			PLASTIC	
94						4		SCREW			#6 x 3/8, FIL	
95						8		WASHER			#6, FLAT	
96						9		WASHER			#6, STAR-LOCK	
97						9		NUT			#6, HEX	
98						1		SCREW			#4, 5/8, FIL	
99						5		SCREW			#4 x 3/8, FIL	
100						12		WASHER			#4, FLAT	
101						12		WASHER			#4, STAR-LOCK	
102						3		NUT			#4, HEX NUT	
103						1		SCREW			#6 x 1/2 FIL	
104						2		SCREW			#8 x 3/8, FIL	
105						2		WASHER			#8, FLAT	
106						1	6000-0181	PWR CONN		K-A 0303 -NYL	3 PIN POD PWR CONN	
107						2		NUT			#8, KEP NUT	
108						A/R		THERMAL COMPOUND			A/R	

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
109						1		22 AWG			RED, 12 IN LG	
110						1		22 AWG			BLK, 12 IN LG	
111						1		22 AWG			GRN, 12 IN LG	
112						1		22 AWG			GRY, 12 IN LG	
113						A/R		18 AWG			BRN	
114						A/R		18 AWG			RED	
115						A/R		22 AWG			BLK	
116						A/R					ORN	
117						A/R					BRN	
118						A/R					YEL	
119						A/R					GRN	
120						A/R		18 AWG			BLU	
121						1		22 AWG	J		OSCILLATOR JUMPER	
122						A/R		18 AWG	XFMR, PIN 7		VIO	
123						A/R		18 AWG	XFMR, PIN 8		GRY	
124						A/R		18 AWG	XFMR, PIN 9		WHT	
125						1	6200-0021	TERMINAL STRIP		NATIONAL TEL-TRONICS	#1131	
126						1	7100-0049	PWR CORD		BELDEN #17251-6		
127						1	7000-0259	STRAIN RELIEF		HAYCO SR-5N-4		
128						4	0920-0036	REAR FOOT				
129						4	—	SCREW			#6-32 x 1 3/8" LG	
130						1	1700-0046	VOLT. REG.	VR3	LM 323 KC		
131						1	6200-0022	SOLDER LUG		HH SMITH #1488-8		
132						1	6000-0041	TEST JACK			BLK	
133						1	7000-0285	GND LUG		HH SMITH 1414-6		
134						1	—	SCREW			4-40 x 1/4 FIL	
135						16	—	WASHER			B.N.C. LOCK	
136						1	7000-0077	GND LUG			B.N.C.	
137												
138												
139						4	—	NUT			#4 SM. PAT. HEX	
140						1	7300-0002	FUSE			3AG 250V SLOW BLOW	
141						4	6100-0015	CABLE CLIP	J1,2,4,5		14 PIN CABLE	
142						1	6100-0020	CABLE CLIP	J3		16 PIN CABLE	
143												
144						4	—	WASHER			#10 STEEL	

Bail Assembly

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						2	0920-0032	END CAP				
2						1	0920-0031	BAIL				
3						1	0920-0030	RUBBER GRIP				
4						4	7000-0300	"PLASTITE" SCREW		FEDERAL SCREW 40301	#4-40 X 3/8 FLAT HEAD TYPE A THREAD	
5						2	7000-0299	WASHER		FEDERAL SCREW 97314	.140 I.D. .500 O.D. .065 THK.	
6						2	—	PAN HEAD SCREW			#6-32 X 1/2 LONG	
7						2	7000-0283	INSERT		E Z LOK 240-006	#6-32 PRESS IN	

MP MASTER
MA34610